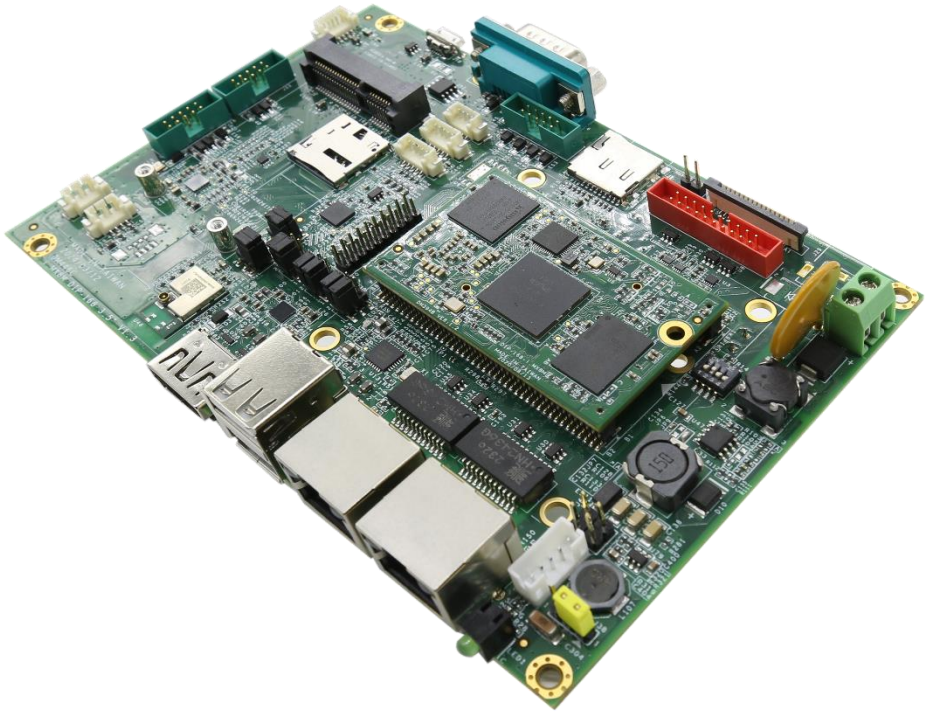
User Manual



NX8MM-35

NXP IMX8M MINI
3.5” SBC

Version 2.0

ICOP Technology Inc.

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Revision History

Revision	Date	Remark
1.0	Nov 1, 2023	First release.
2.0	May 31, 2024	C version release Main difference: MIPI-DSI -> LVDS
R1	June 20, 2024	Connector & Jumper modification

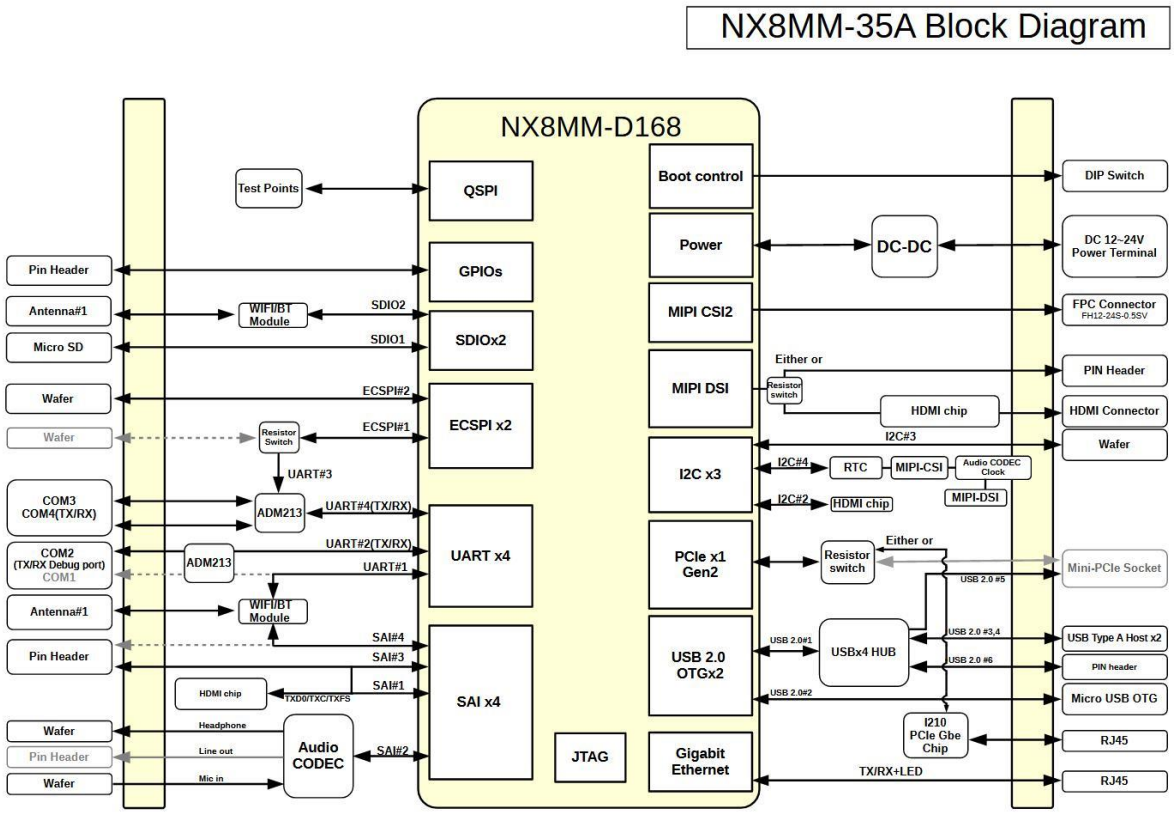
Table of Contents

1 General Information

1.1 Overview

The NX8MM-35 board, measuring 146 x 111 mm and designed in a 3.5" form factor, serves as a platform for the development of the NX8MM-D168 module or can be employed in industrial applications as an ARM-based industrial computing system.

1.2 Block diagram



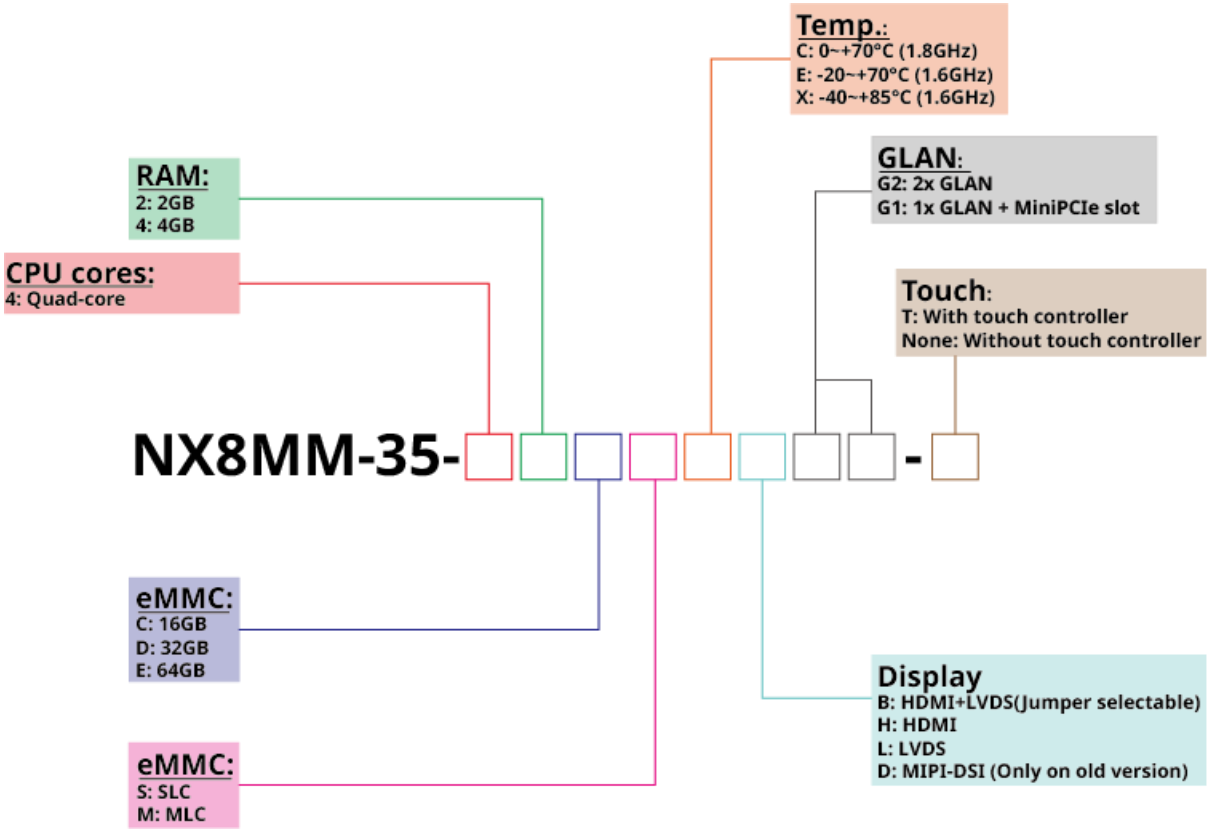
(Line/word in gray means option or not the default setting)

For more detail about selecting I/O function, please refer to Chapter 3.1.2

1.3 Specifications

Processor	NXP i.MX 8M Mini: Up to 4 × Cortex-A53 1.6/1.8GHz 1 × Cortex-M4
Cache	L2: 512KB
System Memory	2/4GB LPDDR4 onboard
Video Decode	1080p60 H.265, H.264, VP8/9
Video Encode	1080p60 H.264, VP8
Display and Camera	HDMI: Maximum resolution up to 1920x1080 @ 60Hz MIPI-DSI 4 lanes up to 1080p60 (Optional to HDMI) LVDS: 24-bit maximum resolution up to 1920 x 1080 @ 60Hz
Storage	eMMC up to 64GB (16GB as default)
Network	Giga LAN x2 (1 can be optional to MiniPCIe slot)
Audio	WM8962B
I/O	USB (ver. 2.0) x4 (1 Micro USB for OTG) COM x2~4 (RS232/RS485) optional to WiFi/BT & SPI Bus i2c x1 SPI x1 (optional between COM3) MiniPCIe x1 (optional between GLAN2) Wi-Fi & Bluetooth 15-bit GPIO x1
Power Requirement	Wide Voltage +12V~24V @ 220 mA (typical)
Weight	170g
Dimensions	146 x 111 mm
Operating Temp.	-20℃ ~ +70℃ -40℃ ~ +85℃ (optional)
Operating System Support	- Yocto Linux - Android

1.4 Ordering Information



2 Hardware Components

2.1 NXP i.MX8MMINI

2.1.1 Overview

i.MX8M MINI is a processor under the i.MX8 family, and it focuses on the video and audio experience. Implementing a quad Arm® Cortex®-A53 1.6GHZ core and a general-purpose Cortex®-M4 400Mhz core processor for low-power processing, the i.MX8M MINI provides excellent experience in multiple industrial applications.

2.1.2 Arm Cortex-A53 MPCore™ Platform

- Quad symmetric Cortex-A53 processors, including:
  - 32 KB L1 Data Cache
  - 32 KB L1 Data Cache
  - Media Processing Engine (MPE) with NEON technology supporting the Advanced Single Instruction Multiple Data architecture:
  - Floating Point Unit (FPU) with support of the VFPv4-D16 architecture
- Support of 64-bit Armv8-A architecture
- 512 KB unified L2 cache
- Target frequency of 1.8GHz

2.1.3 Arm Cortex-M4 platform

- Low power microcontroller available for customer application:
  - low power standby mode
  - IoT features including Weave
  - Manage IR or Wireless Remote
- Cortex M4 CPU:
- 16 KB L1 Instruction Cache
- 16 KB L1 Data Cache
- 256 KB tightly coupled memory (TCM)

2.1.4 System Bus and Interconnect

- Network interconnect (NoC) AXI arbiter.
- Quality of service controller (QoSC) to configure priorities and limits of AXI transcations.
- Performance monitor (PERFMON) to monitor AXI bus activity
- Debug monitor (DBGMON) to record AXI transactions preceding a system reset

2.1.5 Clocking and Resets

- Clock control module (CCM) provides centralized clock generation and control
- Simplified clock tree structure
- Unified clock programming model for each clock root
- Multicore awareness for resource domains
- System reset controller (SRC) provides reset generation and distribution

2.1.6 Interrupts and DMA

- 128 shared peripheral interrupts routed to Cortex-A53 Global Interrupt Controller (GIC) and Cortex-M4 nested vector interrupt controller (NVIC) for flexible interrupt handling
- Three Smart direct memory access (SDMA) engines. Although these three engines are identical to each other, they are integrated into the processor to serve different peripherals.
    - SDMA-1 is a general-purpose DMA engine which can be used by low speed peripherals including UART, SPI and also others peripherals.
    - SDMA-2 and SMDA-3 is used for audio interface, including SAI-1/2/3/5/6, SPDIF and PDM audio input.

2.1.7 On-Chip Memory

- The on-chip memory system consists of the following:
    - Boot ROM (256KB)
    - On-chip RAM (256KB + 32KB)

2.1.8 External Memory Interface

- 32/16-bit DRAM interfaces:
  - LPDDR4 (up to 1.5 GHz)
- 8-bit NAND-Flash, including support for Raw MLC/SLC devices, BCH ECC up to 62-bit, and ONFi3.2 compliance (clock rates up to 100 MHz and data rates up to 200MB/sec)
- eMMC 5.1 Flash (2 interfaces)
- SPI NOR Flash (3 interfaces)
- FlexSPI with support for XIP (for ME in low-power mode) and parallel read mode of two identical FLASH devices

2.1.9 Timers

- One local generic timer integrated into each Cortex-A53 CPU
- Global system counter with timer bus interface to Cortex-A53 MPCore generic timers
- One local system timer (SysTick) integrated into the Cortex-M4 CPU
- Six general purpose timer (GPT) modules
- Three watchdog timer (WDOG) modules
- Four pulse width modulation (PWM) modules

2.1.10 VPU

- 1080p60 VP9 Profile 0, 2 (10-bit)
- 1080p60 HEVC/H.265 Decoder
- 1080p60 AVC/H.264 Baseline, Main, High decoder
- 1080p60 VP8
- 1080p60 AVC/H.264 Encoder
- 1080p60 VP8
- TrustZone support

2.1.11 GPU

- 1080p60 VP9 Profile 0, 2 (10-bit)
- 1080p60 HEVC/H.265 Decoder
- 1080p60 AVC/H.264 Baseline, Main, High decoder
- 1080p60 VP8
- 1080p60 AVC/H.264 Encoder
- 1080p60 VP8
- TrustZone support

2.1.12 Display Interfaces

- LCDIF Display Controller:
  - Supports up to 2 layers of overlay
  - Support up to 1080p60 display through MIPI DSI
- MIPI Interface:
  - 4-lane MIPI CSI interface
  - 4-lane MIPI DSI interface
- CSI Interface:
  - CSI is a simple camera interface which is used to capture the MIPI CSI input and save the pixels into memory

2.1.13 Audio

- S/PDIF Input and Output, including a Raw Capture input mode
- Five external SAI (synchronous audio interface) modules supporting I2S, AC97, TDM, codec/DSP and DSD interfaces, including one SAI with 8 TX and 8 RX lanes, one SAI with 4 TX and 4 RX lanes, two SAI with 2 TX and 2 RX lanes, and one SAI with 1 TX and 1 RX lanes. Supports over 20 channels of audio subject to I/O limitations.

2.1.14 General Connectivity Interfaces

- One PCI Express (PCIe):
  - Single lane supporting PCIe Gen 2
  - Dual mode operation to function as root complex or endpoint
  - Integrated PHY interface
  - Supports L1 low power substate
- Two USB 2.0 OTG controllers with integrated PHY interface
  - Spread spectrum clock support
- Three Ultra Secure Digital Host Controller (uSDHC) interfaces
  - MMC 5.1 compliance with HS400 DDR signaling to support up to 400 MB/sec
  - SD/SDIO 3.01 compliance with 200 MHZ SDR signaling to support up to 100MB/sec
  - Support for SDXC (extended capacity)
- One Gigabit Ethernet controller with support for EEE, Ethernet AVB and IEEE1588
- Four universal asynchronous receiver/transmitter (UART) modules
- Four I2C modules
- Three SPI modules

2.1.15 Security

- RDC – Resource Domain Controller:
  - Supports 4 domains and up to 8 regions
- Arm TrustZone including the TZ architecture:Integrated PHY interface
  - ARM Cortex-A53 MPCore TrustZone support
- On-chip RAM (OCRAM) secure region protection using OCRAM controller
- High Assurance Boot (HAB)
- Cryptographic Acceleration and Assurance Module (CAAM)
  - Support Widevine and PlayReady content protection
  - Public Key Cryptography (PKHA) with RSA and Elliptic Curve (ECC) algorithms
  - Real-time integrity checker (RTIC)

    - DRM support for RSA, AES, 3DES, DES
    - Side channel attack resistance
    - True random number generation (RNG)
    - Manufacturing protection support
- Secure Non-Volatile Storage (SNVS), including
    - Secure Real Time Clock (SRTC)
- Secure JTAG Controller (SJC)

2.1.16 Multicore Support

- Resource domain controller (RDC) to support isolation and safe sharing of system resources
- Messaging unit (MU)
- Hardware Semaphore (SEMA42)
- Shared bus topology

2.1.17 GPIO and Pin Multiplexing

- General-purpose input/output (GPIO) modules with interrupt capability
- Input/output multiplexing controller (IOMUXC) to provide centralized pad control

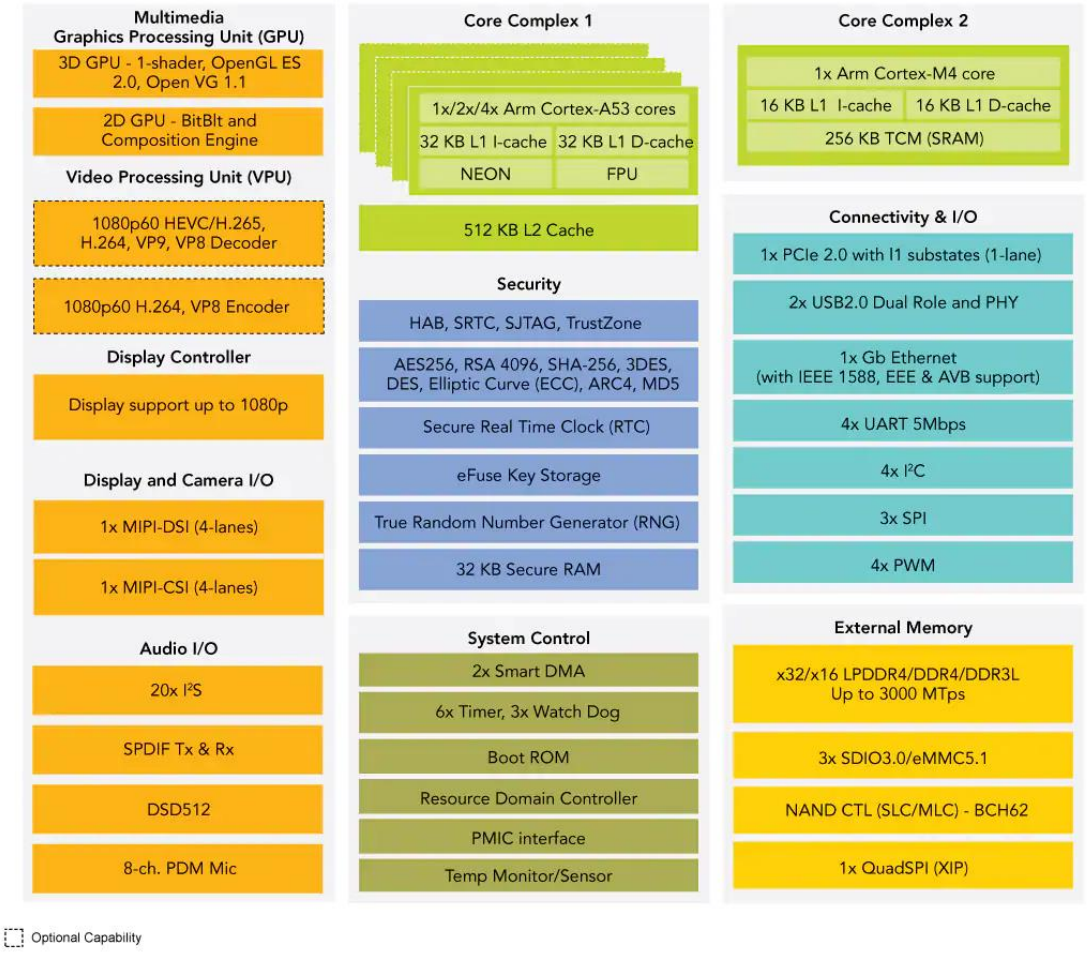
2.1.18 Power Management

- Temperature sensor with programmable trip points
- Flexible power domain partitioning with internal power switches to support efficient power management

2.1.19 System Debug

- ARM CoreSight debug and trace architecture
- Trace Port Interface Unit (TPIU) to support off-chip real-time trace
- Embedded Trace FIFO (ETF) with 4 KB internal storage to provide trace buffering
- Unified trace capability for Quad Cortex-A53 and Cortex-M4 CPUs
- Cross Triggering Interface (CTI)
- Support for 5-pin (JTAG) debug interfaces

2.1.20 i.MX8M MINI Block Diagram

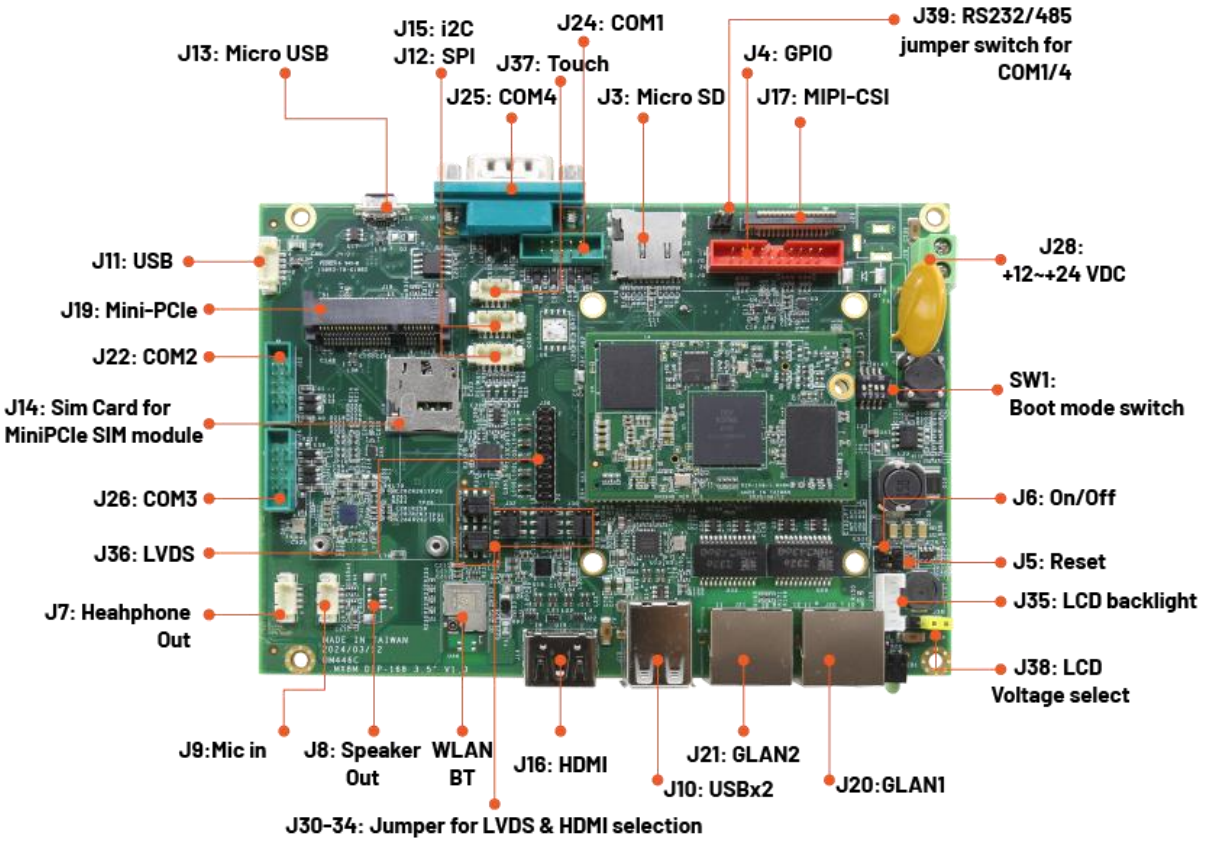


Source: NXP official website

3 Board Outline

3.1 Pin Assignments & switch setting

3.1.1 Board Outline

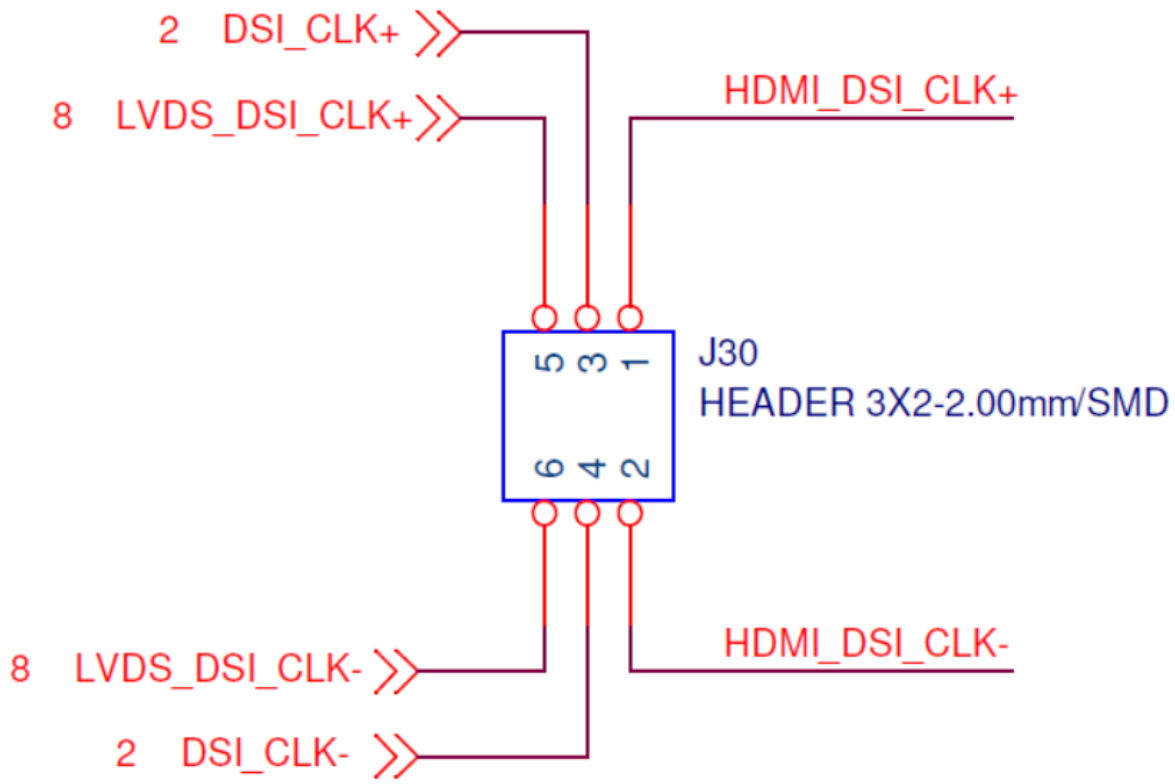


3.1.2 Resistor switch setting

- LVDS or HDMI can be selected using jumper (Depends on the P/N).

Display Setup				
Connector	**Pin 1 – 3**	**Pin 2 - 4**	**Pin 3 - 5**	**Pin 4 - 6**
JP30	HDMI	HDMI	LVDS	LVDS
JP31				
JP32				
JP33				
JP34				
JP35				

*Jumper sample:



- LCD Backlight switch

Connector	Pin 1 + 2	Pin 2 + 3
JP38	+12V	+5V

- COM 1 & 4 RS232/485 select switch

Connector	Pin 1 + 2	Open
JP39	RS485 mode	RS232 mode

- GLAN2 or MINIPCIe can be selected using resistors (Default: GLAN2).

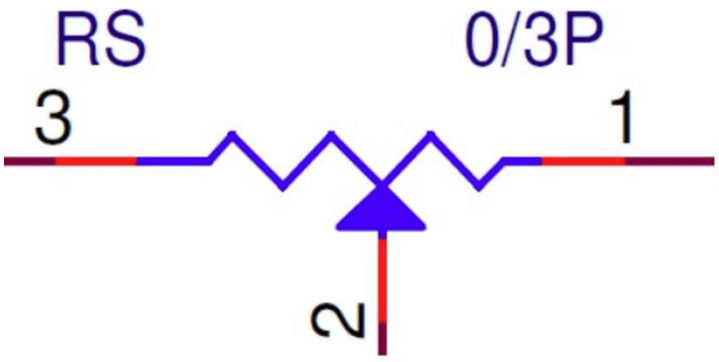
Resistor list	Pad 1 + 2 connected	Pad 2 + 3 connected
RS49~54	MINIPCIe	GLAN2 (Default)

- Wi-Fi/BT or COM1 can be selected using resistors (Default: Wi-Fi/BT).

Resistor list	Pad 1 + 2 connected	Pad 2 + 3 connected
RS3/4/6/8	Wi-Fi/BT (Default)	COM1

- COM3 or SPI1 can be selected using resistors (Default: COM3).

Resistor list	Pad 1 + 2 connected	Pad 2 + 3 connected
RS5/7/9/10	COM3 (Default)	SPI1



3.2 Connector and Jumper Summary

Nbr.	Name	Type	Number of pins
J2/3	Micro SD card slot		
J4	GPIO	Pin header, 2.0mm, 2x10	20
J5	H/W Reset	Pin header, 2.0mm, 2x1	2
J6	On/Off	Pin header, 2.0mm, 2x1	2
J7	Headphone Out	Wafer, 1.25mm, 4x1	4
J8	Speaker Out(optional)	Wafer, 1.25mm, 4x1	4
J9	Mic In	Wafer, 1.25mm, 4x1	4
J10	USB3/4	Type A USB Connector	12
J11	USB5	Wafer, 1.25mm, 5x1	5
J12	SPI1 Pin header	Wafer, 1.25mm, 5x1	5
J13	USB1	Micro USB Connector	9
J14	Micro SIM Socket	Micro SD Socket	18
J15	I2C3 Pin header	Wafer, 1.25mm, 5x1	5
J16	HDMI Out	HDMI connector	23
J17	MIPI-CSI	Wafer, 1.0mm, 15x1	15
J19	MINIPCI-EXP	Standard Mini PCI Express Connector	52
J20	GLAN1	RJ45 Connector	12
J21	GLAN2	RJ45 Connector	12
J22	COM2 RS232 (Debug port)	Pin Header, 2.0mm, 5x2	10
J24	COM1 RS232/485	Pin Header, 2.0mm, 5x2	10
J25	COM4 RS232/485	D-Sub Male	9
J26	COM3 RS232 (TTL Option)	Pin Header, 2.0mm, 5x2	10
J28	Power connector	Terminal Block, 5.0mm, 2x1	2
J29	5V Power Jack(Option)	Power DC jack	3
J30-34	HDMI/LVDS Jumper	Pin Header, 2.0mm, 2x3	6
J35	LCD backlight	Pin Header, 2.0mm, 1x5	5
J36	LVDS	Pin Header, 2.0mm, 2x10	20

J37	Touch screen	Wafer, 1.25mm. 1x4	4
J38	LVDS backlight voltage select	Pin Header, 2.0mm, 1x3	3
J39	RS232/485 Jumper Switch for COM 1 & 4	Pin Header, 2.0mm, 2x1	2

3.3 Signal Description

J4: GPIO pins

PIN#	Function	TYPE	Description
1	N/C		
2	VCC3	3.3V	
3	GPIO	3.3V	GPIO1_15
4	GPIO	3.3V	Originally SAI1_RXC signal
5	GPIO	3.3V	Originally SAI3_RXC signal
6	GPIO	3.3V	Originally SAI1_MCLK signal
7	GPIO	3.3V	Originally SAI3_RXD signal
8	GPIO	3.3V	Originally SAI1_RXD0 signal
9	GPIO	3.3V	GPIO1_01
10	GPIO	3.3V	GPIO4_21
11	GPIO	3.3V	GPIO1_07
12	GPIO	3.3V	GPIO4_22
13	GPIO	3.3V	GPIO5_2; NC if enable LCD_BS
14	GPIO	3.3V	GPIO4_31
15	NC		
16	GPIO	3.3V	Originally SAI5_MCLK
17	GPIO	3.3V	GPIO5_5; NC if enable LCD_BL
18	GPIO	3.3V	SAI5_RXFS
19	GND		
20	GND		

J5: Hardware reset pins

PIN#	Function
1	RST_CORE
2	GND

J6: On/Off pins

PIN#	Function
1	On_Off
2	GND

J7: Headphone connector

PIN#	Function
1	HP_LEFT2_O
2	GND_AUD
3	GND_AUD
4	HP_RIGHT2_O

J8: Speaker out connector

PIN#	Function
1	SPK_LP2_O
2	SPK_LN2_O
3	SPK_RP2_O
4	SPK_RN2_O

J9: Mic-in connector

PIN#	Function
1	MICBIAS
2	GND_AUD
3	GND_AUD
4	MIC_IN

J10: USB 3/4

PIN#	Function	PIN#	Function
1	VCC	5	VCC
2	LUSBD4-	6	LUSBD3-
3	LUSBD4+	7	LUSBD3+
4	GND	8	GND
H3	FGND	H1	FGND
H4	FGND	H2	FGND

J11: USB5

PIN#	Function
1	VCC
2	LUSBD5-
3	LUSBD5+
4	GND
5	FGND

J13: Micro USB (USB1)

PIN#	Function
1	VCC
2	LUSBD1-
3	LUSBD1+
4	USB1_ID
5	GND
6	FGND
7	FGND
8/9	NC
H1	FGND
H2	FGND

J12: SPI1

PIN#	Function	TYPE	Description
1	SPI1_CLK_R	3.3V	NC if using UART3 for COM3
2	SPI1_MOSI_R	3.3V	NC if using UART3 for COM3
3	SPI1_MISO_R	3.3V	NC if using UART3 for COM3
4	SPI1_SS_R	3.3V	NC if using UART3 for COM3
5	GND		

J14: Micro SIM socket

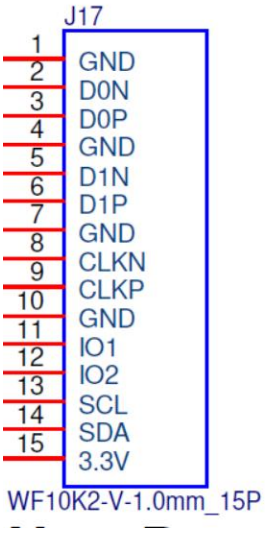
PIN#	Function
1	SIM-VCC
2	SIM-RST
3	SIM-CLK
4	GND
5	SIM-VPP
6	SIM-IO
7	NC
8~17	GND
18	NC

J15: I2C3

PIN#	Function	Type
1	I2C3_SCL	3.3V
2	I2C3_SDA	3.3V
3	NC	
4	NC	
5	GND	

J17: MIPI-CSI

PIN#	Function	PIN#	Function
1	GND	9	CSI_CLK+
2	CSI_D0-	10	GND
3	CSI_D0+	11	CSI_IO_3V3
4	GND	12	NC
5	CSI_D1-	13	CAMERA_SCL
6	CSI_D1+	14	CAMERA_SDA
7	GND	15	VCC 3.3V
8	CSI_CLK-		



J20: LAN- RGMII

PIN#	Function	PIN#	Function	PIN#	Function
1	GTX+	6	GRX-	11	GND
2	GTX--	7	GRXD+	12	LED_ACT
3	GRX+	8	GRXD--	H1	FGND
4	GRXC+	9	LED_LINK10_100+	H2	FGND
5	GTXC-	10	LED_LINK1000		

J21: LAN- RGMII

PIN#	Function	PIN#	Function	PIN#	Function
1	GTX+	6	GTXC-	11	LED_ACT_R
2	GTX--	7	GRXD+	12f	VCC
3	GRX+	8	GRXD--	H1	FGND
4	GRX-	9	LED_LINK1000_R	H2	FGND
5	GTXC+	10	LED_100_R		

J24: COM1

PIN#	Function
1	NC
2	RXD1
3	TXD1
4	NC
5	GND
6	NC
7	RTS1
8	CTS1
9	NC
10	VCC(option)

J22: COM2 (Debug port)

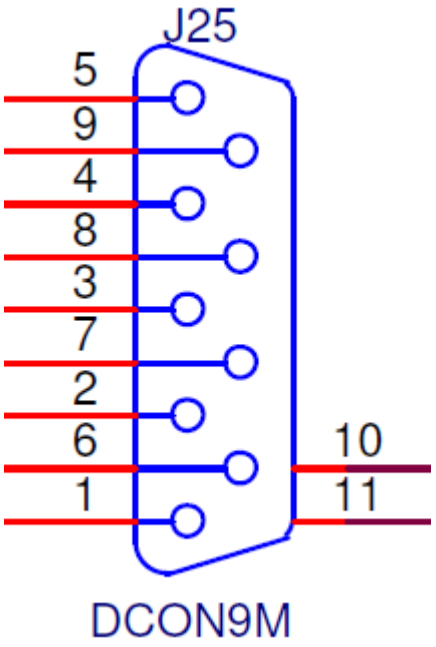
PIN#	Function
1	NC
2	RXD2
3	TXD2
4	NC
5	GND
6	NC
7	NC
8	NC
9	NC
10	NC

J22: COM3

PIN#	Function
1	NC
2	RXD3
3	TXD3
4	NC
5	GND
6	NC
7	RTS3
8	CTS3
9	NC
10	VCC(option)

J25: COM4

PIN#	Function
1	NC
2	RXD4
3	TXD4
4	RS485+
5	GND
6	RS485-
7	NC
8	NC
9	NC
10	FGND
11	FGND



J28: Power 12-24V

PIN#	Function
1	PWR+
2	PWR-

J29: Power jack 5V (Optional)

PIN#	Function
1	VCC
2	GND
3	NC

J30: HDMI/LVDS Jumper

PIN#	Function	PIN#	Function
1	HDMI_DSI_CLK+	4	DSI_CLK-
2	HDMI_DSI_CLK-	5	LVDS_DSI_CLK+
3	DSI_CLK+	6	LVDS_DSI_CLK-

J31: HDMI/LVDS Jumper

PIN#	Function	PIN#	Function
1	HDMI_DSI_D0+	4	DSI_D0-
2	HDMI_DSI_D0-	5	LVDS_DSI_D0+
3	DSI_D0+	6	LVDS_DSI_D0-

J32: HDMI/LVDS Jumper

PIN#	Function	PIN#	Function
1	HDMI_DSI_D1+	4	DSI_D1-
2	HDMI_DSI_D1-	5	LVDS_DSI_D1+
3	DSI_D1+	6	LVDS_DSI_D1--

J33: HDMI/LVDS Jumper

PIN#	Function	PIN#	Function
1	HDMI_DSI_D2+	4	DSI_D2-
2	HDMI_DSI_D2-	5	LVDS_DSI_D2+
3	DSI_D2+	6	LVDS_DSI_D2--

J34: HDMI/LVDS Jumper

PIN#	Function	PIN#	Function
1	HDMI_DSI_D3+	4	DSI_D3-
2	HDMI_DSI_D3-	5	LVDS_DSI_D3+
3	DSI_D3+	6	LVDS_DSI_D3-

J35: LCD backlight

PIN#	Function
1	+12V/+5V
2	GND
3	Backlight
4	Brightness
5	GND

J38: LVDS backlight voltage select

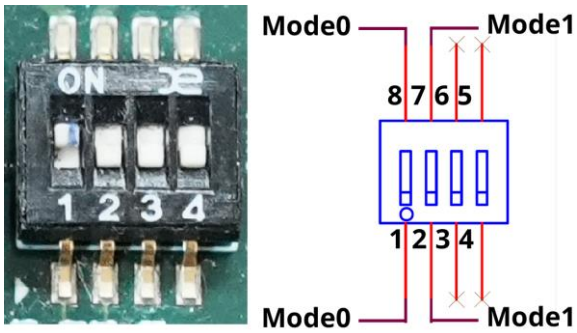
PIN#	Function
1	+12V
2	LCD backlight Pin
3	+5V

J39: COM1&4 RS232/485 selection

PIN#	Function
1	RS485 Enable
2	GND

Boot Mode (2pins)

PIN#	Function	TYPE	Description
B60	BOOT_MODE0	I	**BOOT_MODE0**
B62	BOOT_MODE1	I	**BOOT_MODE1**



Function	Mode 0	Mode 1
Internal Boot Mode	Set to 1 position	Set to 7 position
Serial Download Mode (For writing image by micro USB only)	Set to 8 position	Set to 2 position

J36: LVDS pins

PIN#	Function	TYPE	Description
1	VCC3	3.3V	
2	VCC3	3.3V	
3	GND		
4	GND		
5	LA0P	P	LVDS data output 0
6	LA0N	N	LVDS data output 0
7	LA1N	N	LVDS data output 1
8	GND		
9	GND		
10	LA1P	P	LVDS data output 1
11	LA2P	P	LVDS data output 2
12	LA2N	N	LVDS data output 2
13	LCKN	N	LVDS clock
14	GND		
15	GND		
16	LCKP	P	LVDS clock
17	LA3N	N	LVDS data output 3
18	GND		
19	GND		
20	LY3P	P	LVDS data output 3

J37: Touch screen connector

PIN#	Function
1	Y-
2	X-
3	Y+
4	X+

4 Software Resources

4.1 ICOP Wiki

ICOP Technology has a wiki site which provides all of the software support for NX8MM-35 such as demo image, recipe, and testing method.
Please check the following link:
https://wiki.icop.com.tw/product/index.php/NX8MM-35

If you did not find the resources you need on the wiki site, please contact info@icop.com.tw or your ICOP sales representative.

Warranty

This product is warranted to be in good working order for a period of one year (12 months) from the date of purchase. Should this product fail to be in good working order at any time during this period, we will, at our option, replace or repair it without additional charge except as set forth in the following terms. This warranty does not apply to products damaged by misuse, modifications, accident or disaster. Vendor assumes no liability for any damages, lost profits, lost savings or any other incidental or consequential damage resulting from the use, misuse of, originality to use this product. Vendor will not be liable for any claim made by any other related party. Return authorization must be obtained from the vendor before returned merchandise is accepted. Authorization can be obtained by calling or faxing the vendor and requesting a Return Merchandise Authorization (RMA) number. Returned goods should always be accompanied by a clear problem description. Should you have questions about warranty and RMA service, please contact us directly.

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