

## 碩擇實業股份有限公司 GOOD CHOICE ENTERPRISE CO., LTD



## **Disea Electronics Co., LTD**

TO: 瞻營全電子股份有限公司

**DATE: AUG.08-2019** 

TFT LCM

## **ZW-T090BAE-02**

Approved By	Comment

PREPARED	CHECKED	VERIFIED BY QA DEPT	VERIFIED BY R&D DEPT
YGM	Tim		Paul

客戶確認:			

Version :1 Page:1/18



# PRODUCT SPECIFICATIONS

For Cu	stomer:		☐ : APPF	ROVAL F	OR SPECIFICATION
Custor	ner Model N	lo	□ : APP	ROVAL F	OR SAMPLE
Modul	e No.:	ZW-T090BAE-02	<u>Date</u>	: 2019-0	08-08
Table of Cont	ents				
No.		Item			Page
1	Cover Shee	et(Table of Contents)			P1
2	Revision R	ecord			P2
3	General Sp	ecifications			P3
4	Outline Dra	awing			P4
5	Absolute M	laximum Ratings		***	P5
6	Electrical S	pecifications			P6-P11
7	Optical Cha	aracteristics		-	P12-P15
8	Reliability '	Test Items and Criteria			P16
9	Precaution	s for Use of LCD Modules			P17-P18
For Custom	er's Accep	tance:			
Approv	ed By		Commen	t	
PREPA	RED	CHECKED	VERIFIED BY QA	DEPT	VERIFIED BY R&D DEPT
YG	M	Tim			Paul



### 2. Revision Record

		<u> </u>		
Date	Rev.No.	Page	Revision Items	Prepared
2019-07-30	V0		The first release	YGM
2019-08-08	V1		Updated Item #4	CJ Jiang



### 3. General Specifications

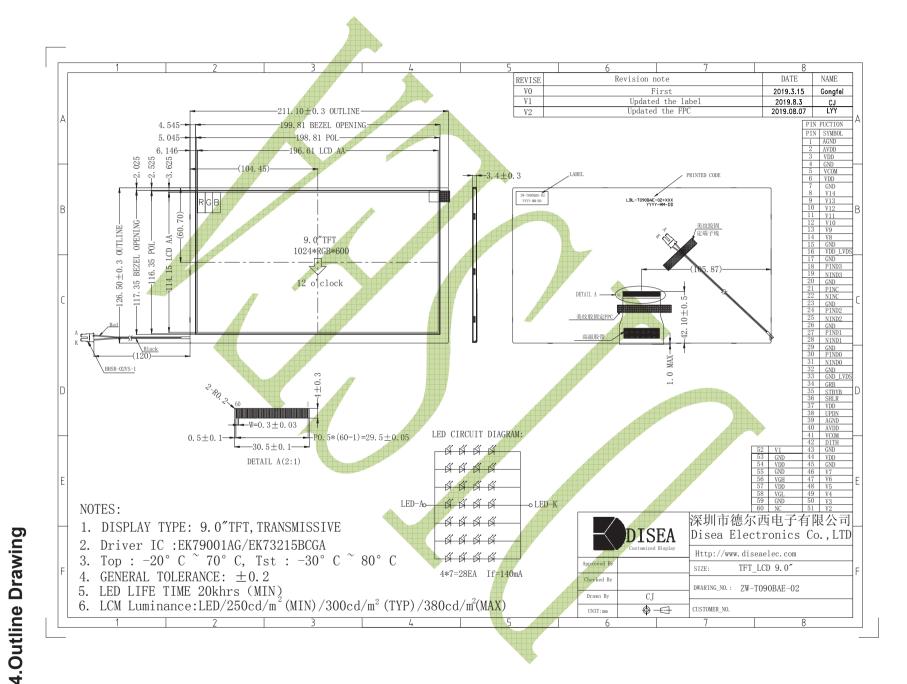
ZW-T090BAE-02 is a TFT-LCD module. It is composed of a TFT-LCD panel, driver IC, FPC, a back light unit. The 9.0" display area contains 1024x(RGB)x600 pixels and can display up to 16.7M colors. This product accords with RoHS environmental criterion.

Item	Contents	Unit	Note
LCD Type	TFT	-	
Display color	16.2M	-	1
Viewing Direction	12	O'Clock	
Gray scale inversion direction	6	O'Clock	
Operating temperature	-20~+70	°C	
Storage temperature	-30~+80	°C	
Module size	211.10X126.50X3.4	mm	2
Active Area(W×H)	196.61x114.15	mm	•
Number of Dots	1024×600	dots	
TFT Controller	EK79001AG+EK73215BCGA	_	
CTP driver	NA	-	
Power Supply Voltage	3.3	V	
Backlight	4S7P-LEDs (white)	pcs	
Weight	185	g	
Interface	LVDS	-	

Note 1: Color tune is slightly changed by temperature and driving voltage.

Note 2: Without FPC, Wire and Solder.





### 5. Absolute Maximum Ratings(Ta=25 °C)

#### 5.1 Electrical Absolute Maximum Ratings.(Vss=0V, Ta=25°C)

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VDD	-0.3	5.0	V	1, 2
	AVDD	-0.5	14.85	V	1, 2
	VGH	-0.3	+42	V	1, 2
	VGL	-20	0.3	V	1, 2

#### Notes:

- 1. If the module is above these absolute maximum ratings. It may become permanently damaged. Using the module within the following electrical characteristic conditions are also exceeded, the module will malfunction and cause poor reliability.
- 2.  $V_{DVDD} > V_{SS}$  must be maintained.
- 3. Please be sure users are grounded when handing LCD Module.

#### 5.2 Environmental Absolute Maximum Ratings.

**************************************			Contraduct.	Honotons, Anonor	
Item	Stor	age	Operat	Note	
	MIN.	MAX.	MIN.	MAX.	NOIC
Ambient Temperature	-30°C	80°C	-20°C	70°C	1,2
Humidity	1	-	1	-	3

- 1. The response time will become lower when operated at low temperature.
- 2. Background color changes slightly depending on ambient temperature.

The phenomenon is reversible.

3. Ta<=40 °C:85%RH MAX.

Ta>=40 °C:Absolute humidity must be lower than the humidity of 85%RH at 40 °C.

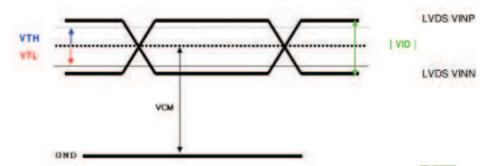
## 6. Electrical Specifications and Instruction Code

### 6.1 Electrical characteristics(Vss=0V ,Ta=25 $^{\circ}$ C)

Item	Symbol	Min	Тур	Max	Unit	Note
Power supply	VDD	3.0	3.3	3.6	V	
	VCM	0.5* VID	-	2.4-0.5* VID	V	Note1
Logic Input	VID	200		600	mV	Note1
voltage	VTH	-	-	100	mV	VCM=1.2V Note1
	VTL	-100	1	-	mV	
Analog Power Supply Voltage	AVDD	10.4	10.8	11.2	V	
Gate On Power Supply Voltage	VGH	17	18	19	V	
Gate Off Power Supply Voltage	VGL	-9	-8	-7	V	
Common Power Supply Voltage	VCOM	3.95	4.25	4.55	V	Note2
	V1	-	8.54	-	V	
	V2	-	8.43		V	
	V3	-	6.94	-	V	
	V4	-	6.48	-	V	
	V5	-	6.16	-	V	
	V6		5.79	-	V	
Gamma Voltage	V7		5.70	-	V	
	V8		3.32	-	V	
	V9	-	3.22 2.66	-	V	
	V10 V11	-	2.00	-	V	
	V11	-	1.75	<u>-</u>	V	
	V12	<u>-</u>	0.27	-	V	
	V14	-	0.22	_	V	



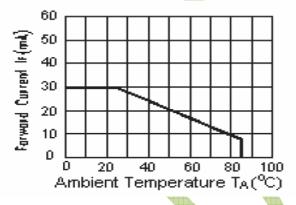
Note: 1: LVDS signal



Note: 2: Please adjust VCOM to make the flicker level be minimum.

### 6.2 LED backlight specification(VSS=0V,Ta=25°C)

Item	Symbol	Condition	Min	Тур	Max	Unit	Note
10111	Cy.moor	Schallon		. 70	max	O/III	1,1010
Supply voltage	$V_{f}$	lf=140mA	10.8	13.2	14.4	V	
Uniformity	∆Вр	If=140mA	75	80	-	%	
Life Time	time	If=140mA	20K		-	hours	1



Note 1: Brightness to be decreased to 50% of the initial value at ambient temperature TA=25  $^{\circ}C$ 

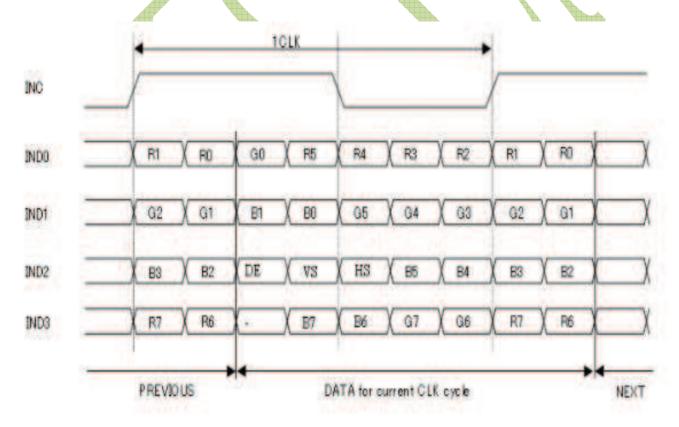


#### 6.3 input Timing table

#### 6.3.1 Timing Specification

<u> </u>	IT	EM		SYMBOL	MIN	TYP	MAX	UNIT
LVDS input signal sequence		CLK Fre	quency	tclk	45	51.2	57	MHz
		Horizontal total Time	t <sub>H</sub>	1324	1344	1364	tCLK	
LCD input signal		Horizontal	Horizontal effective Time	t <sub>HA</sub>	1024		tCLK	
sequence (Input LVDS	DENA		Horizontal Blank Time	t <sub>HB</sub>	300	320 ^	340	tCLK
Transmitter)		Vertical	Vertical total Time	t <sub>V</sub>	625	635	645	t <sub>H</sub>
Transmitter)			Vertical effective Time	t <sub>VA</sub>	600			t <sub>H</sub>
			Vertical Blank Time	t <sub>VB</sub>	25	35	45	t <sub>H</sub>

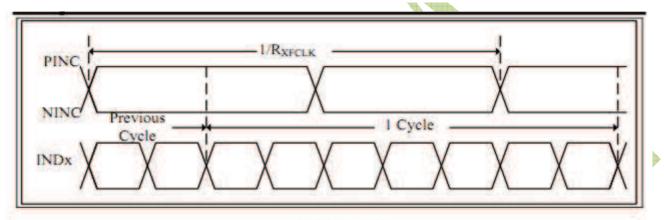
#### 6.3.2 LVDS Input Data mapping



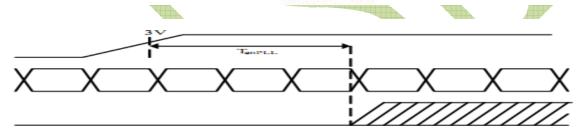


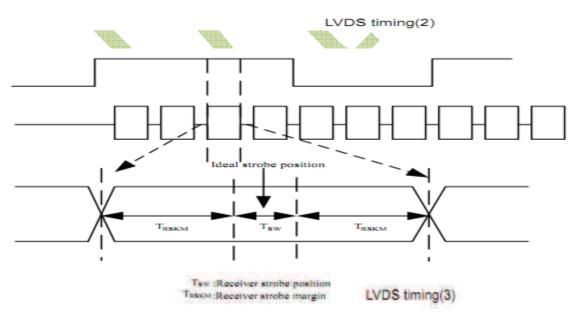
#### **6.4 AC Characteristics**

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
Clock Frequency	RxFCLK		20	-	71	MHz
Input data skew margin	TRSKM	VID =400mV RxVCM=1.2V RxFCLK=71MHz	500			ps
Clock High Time	TLVCH			4/(7* RxFCLK)		ns
Clock High Time	TEVOR			4/(/ KXFCLK)		ns
Clock Low Time	TLVCL			3/(7* RxFCLK)		ns
PLL wake-up-time	TenPLL				150	us



LVDS timing(1)







### 6.3 Interface signals

Pin No.	Symbol	I/O	Function	
1	AGND	Р	Analog ground	
2	AVDD	Р	Analog power	
3	VDD	Р	Digital power	
4	GND	Р	Digital ground	
5	VCOM	Р	Common voltage	
6	VDD	Р	Digital power	
7	GND	Р	Digital ground	
8	V14	Р	Gamma correction voltage reference	
9	V13	Р	Gamma correction voltage reference	
10	V12	Р	Gamma correction voltage reference	
11	V11	Р	Gamma correction voltage reference	
12	V10	Р	Gamma correction voltage reference	
13	V9	Р	Gamma correction voltage reference	
14	V8	Р	Gamma correction voltage reference	
15	GND	P	Digital ground	
16	VDD_LVDS	Р	LVDS powe	
17	GND	Р	Digital ground	
18	PIND3	Ι	Positive LVDS differential data inputs	
19	NIND3		Negative LVDS differential data inputs	
20	GND	P	Digital ground	
21	PINC	ı	Positive LVDS differential clock inputs	
22	NINC	I	Negative LVDS differential clock inputs	
23	GND	Р	Digital ground	
24	PIND2		Positive LVDS differential data inputs	
25	NIND2		Negative LVDS differential data inputs	
26	GND	Р	Digital ground	
27	PIND1	Ι	Positive LVDS differential data inputs	
28	NIND1		Negative LVDS differential data inputs	
29	GND	P	Digital ground	
30	PIND0	I	Positive LVDS differential data inputs	
31	NIND0	I	Negative LVDS differential data inputs	
32	GND	Р	Digital ground	
33	GND_LVDS	Р	LVDS ground	
			Global reset pin. Active low to enter reset state.	
34	GRB	I	Suggest to connecting with an RC reset circuit for stability.	
			Normally pull high. (R=10 $K_{\Omega}$ , C=0.1 $\mu$ F)	



Standby mode, normally pull high STBYB=" 1" , normal operation STBYB=" 0" , timing control, source driver will turn off, all output are high-Z  36 SHLR I Left or right display control  37 VDD P Digital power  38 UPDN I Up / down display control  39 AGND P Analog ground  40 AVDD P Analog power  41 VCOM P Common voltage  Dithering function enable control.Normally pull high. DITHB=1, enable disable internal dithering function. DITHB=1, enable disable internal dithering function. DITHB=0, disable internal dithering function. DITHB=0 Digital ground  44 VDD P Digital ground  45 GND P Digital ground  46 V7 I Gamma correction voltage reference  47 V6 I Gamma correction voltage reference  48 V5 I Gamma correction voltage reference  49 V4 I Gamma correction voltage reference  50 V3 I Gamma correction voltage reference  51 V2 I Gamma correction voltage reference  52 V1 I Gamma correction voltage reference  53 GND P Digital ground  54 VDD P Digital ground  55 GND P Digital ground  56 VGH P Positive power for TFT  57 VDD P Digital ground for Gate IC  Not connect				-
37 VDD P Digital power  38 UPDN I Up / down display control  39 AGND P Analog ground  40 AVDD P Analog power  41 VCOM P Common voltage  Dithering function enable control Normally pull high.  42 DITH I DITHB=1, enable disable internal dithering function.  DITHB=0, disable internal dithering function.  43 GND P Digital ground  44 VDD P Digital ground  46 V7 I Gamma correction voltage reference  47 V6 I Gamma correction voltage reference  48 V5 I Gamma correction voltage reference  49 V4 I Gamma correction voltage reference  50 V3 I Gamma correction voltage reference  51 V2 I Gamma correction voltage reference  52 V1 I Gamma correction voltage reference  53 GND P Digital ground  54 VDD P Digital ground  55 GND P Digital ground  56 VGH P Positive power for TFT  57 VDD P Digital ground for Gate IC	35	STBYB	I	STBYB=" 1", normal operation STBYB=" 0", timing control, source driver will turn off, all
38 UPDN I Up / down display control  39 AGND P Analog ground  40 AVDD P Analog power  41 VCOM P Common voltage  Dithering function enable control Normally pull high.  42 DITH I DITHB=1, enable disable internal dithering function.  DITHB=0, disable internal dithering function.  43 GND P Digital ground  44 VDD P Digital power  45 GND P Digital ground  46 V7 I Gamma correction voltage reference  47 V6 I Gamma correction voltage reference  48 V5 I Gamma correction voltage reference  49 V4 I Gamma correction voltage reference  50 V3 I Gamma correction voltage reference  51 V2 I Gamma correction voltage reference  52 V1 I Gamma correction voltage reference  53 GND P Digital ground  54 VDD P Digital ground  55 GND P Digital power  56 VGH P Positive power for TFT  57 VDD P Digital power for Gate IC  58 VGL P Negative power for TFT  59 GND P Digital ground for Gate IC	36	SHLR	I	Left or right display control
39 AGND P Analog ground 40 AVDD P Analog power 41 VCOM P Common voltage  Dithering function enable control.Normally pull high.  DITHB=1, enable disable internal dithering function.  DITHB=0, disable internal dithering function.  DITHB=1, enable disable internal dithering function.  DITHB=0, disable internal dithering function.  DITHB=1, enable internal dithering function.	37	VDD	Р	Digital power
40 AVDD P Analog power  41 VCOM P Common voltage  Dithering function enable control.Normally pull high.  42 DITH I DITHB=1, enable disable internal dithering function.  DITHB=0,disable internal dithering function.  DITHB=0,disable internal dithering function.  DITHB=0,disable internal dithering function.  43 GND P Digital ground  44 VDD P Digital ground  45 GND P Digital ground  46 V7 I Gamma correction voltage reference  47 V6 I Gamma correction voltage reference  48 V5 I Gamma correction voltage reference  49 V4 I Gamma correction voltage reference  50 V3 I Gamma correction voltage reference  51 V2 I Gamma correction voltage reference  52 V1 I Gamma correction voltage reference  53 GND P Digital ground  54 VDD P Digital ground  55 GND P Digital ground  56 VGH P Positive power for TFT  57 VDD P Digital power for Gate IC  58 VGL P Negative power for TFT  59 GND P Digital ground for Gate IC	38	UPDN	I	Up / down display control
41 VCOM P Common voltage  Dithering function enable control.Normally pull high.  DITHB=1, enable disable internal dithering function.  DITHB=0, disable internal dithering function.  43 GND P Digital ground  44 VDD P Digital Power  45 GND P Digital ground  46 V7 I Gamma correction voltage reference  47 V6 I Gamma correction voltage reference  48 V5 I Gamma correction voltage reference  49 V4 I Gamma correction voltage reference  50 V3 I Gamma correction voltage reference  51 V2 I Gamma correction voltage reference  52 V1 I Gamma correction voltage reference  53 GND P Digital ground  54 VDD P Digital ground  55 GND P Digital ground  56 VGH P Positive power for TFT  57 VDD P Digital power for Gate IC  58 VGL P Negative power for TFT  59 GND P Digital ground for Gate IC	39	AGND	Р	Analog ground
DITH I Dithering function enable control.Normally pull high. DITHB=1, enable disable internal dithering function. DITHB=0, disable internal dithering function. DITHB=0, disable internal dithering function.  43 GND P Digital ground  44 VDD P Digital Power  45 GND P Digital ground  46 V7 I Gamma correction voltage reference  47 V6 I Gamma correction voltage reference  48 V5 I Gamma correction voltage reference  49 V4 I Gamma correction voltage reference  50 V3 I Gamma correction voltage reference  51 V2 I Gamma correction voltage reference  52 V1 I Gamma correction voltage reference  53 GND P Digital ground  54 VDD P Digital ground  55 GND P Digital ground  56 VGH P Positive power for TFT  57 VDD P Digital power for Gate IC  58 VGL P Negative power for TFT  59 GND P Digital ground for Gate IC	40	AVDD	Р	Analog power
42 DITH I DITHB=1, enable disable internal dithering function.  43 GND P Digital ground  44 VDD P Digital Power  45 GND P Digital ground  46 V7 I Gamma correction voltage reference  47 V6 I Gamma correction voltage reference  48 V5 I Gamma correction voltage reference  49 V4 I Gamma correction voltage reference  50 V3 I Gamma correction voltage reference  51 V2 I Gamma correction voltage reference  52 V1 I Gamma correction voltage reference  53 GND P Digital ground  54 VDD P Digital ground  55 GND P Digital ground  56 VGH P Positive power for TFT  57 VDD P Digital ground for Gate IC  58 VGL P Negative power for TFT  59 GND P Digital ground for Gate IC	41	VCOM	Р	Common voltage
44 VDD P Digital Power  45 GND P Digital ground  46 V7 I Gamma correction voltage reference  47 V6 I Gamma correction voltage reference  48 V5 I Gamma correction voltage reference  49 V4 I Gamma correction voltage reference  50 V3 I Gamma correction voltage reference  51 V2 I Gamma correction voltage reference  52 V1 I Gamma correction voltage reference  53 GND P Digital ground  54 VDD P Digital power  55 GND P Digital ground  56 VGH P Positive power for TFT  57 VDD P Digital power for Gate IC  58 VGL P Negative power for Gate IC	42	DITH	I	DITHB=1, enable disable internal dithering function.
45 GND P Digital ground  46 V7 I Gamma correction voltage reference  47 V6 I Gamma correction voltage reference  48 V5 I Gamma correction voltage reference  49 V4 I Gamma correction voltage reference  50 V3 I Gamma correction voltage reference  51 V2 I Gamma correction voltage reference  52 V1 I Gamma correction voltage reference  53 GND P Digital ground  54 VDD P Digital power  55 GND P Digital ground  56 VGH P Positive power for TFT  57 VDD P Digital power for Gate IC  58 VGL P Negative power for Gate IC	43	GND	P	Digital ground
46 V7 I Gamma correction voltage reference  47 V6 I Gamma correction voltage reference  48 V5 I Gamma correction voltage reference  49 V4 I Gamma correction voltage reference  50 V3 I Gamma correction voltage reference  51 V2 I Gamma correction voltage reference  52 V1 I Gamma correction voltage reference  53 GND P Digital ground  54 VDD P Digital power  55 GND P Digital ground  56 VGH P Positive power for TFT  57 VDD P Digital power for Gate IC  58 VGL P Negative power for TFT  59 GND P Digital ground for Gate IC	44	VDD	Р	Digital Power
47 V6 I Gamma correction voltage reference  48 V5 I Gamma correction voltage reference  49 V4 I Gamma correction voltage reference  50 V3 I Gamma correction voltage reference  51 V2 I Gamma correction voltage reference  52 V1 I Gamma correction voltage reference  53 GND P Digital ground  54 VDD P Digital power  55 GND P Digital ground  56 VGH P Positive power for TFT  57 VDD P Digital power for Gate IC  58 VGL P Negative power for Gate IC	45	GND	Р	Digital ground
48 V5 I Gamma correction voltage reference 49 V4 I Gamma correction voltage reference 50 V3 I Gamma correction voltage reference 51 V2 I Gamma correction voltage reference 52 V1 I Gamma correction voltage reference 53 GND P Digital ground 54 VDD P Digital power 55 GND P Digital ground 56 VGH P Positive power for TFT 57 VDD P Digital power for Gate IC 58 VGL P Negative power for TFT 59 GND P Digital ground for Gate IC	46	V7	I	Gamma correction voltage reference
49 V4 I Gamma correction voltage reference 50 V3 I Gamma correction voltage reference 51 V2 I Gamma correction voltage reference 52 V1 I Gamma correction voltage reference 53 GND P Digital ground 54 VDD P Digital power 55 GND P Digital ground 56 VGH P Positive power for TFT 57 VDD P Digital power for Gate IC 58 VGL P Negative power for TFT 59 GND P Digital ground for Gate IC	47	V6		Gamma correction voltage reference
50 V3 I Gamma correction voltage reference 51 V2 I Gamma correction voltage reference 52 V1 I Gamma correction voltage reference 53 GND P Digital ground 54 VDD P Digital power 55 GND P Digital ground 56 VGH P Positive power for TFT 57 VDD P Digital power for Gate IC 58 VGL P Negative power for TFT 59 GND P Digital ground for Gate IC	48	V5	T	Gamma correction voltage reference
51 V2 I Gamma correction voltage reference 52 V1 I Gamma correction voltage reference 53 GND P Digital ground 54 VDD P Digital power 55 GND P Digital ground 56 VGH P Positive power for TFT 57 VDD P Digital power for Gate IC 58 VGL P Negative power for TFT 59 GND P Digital ground for Gate IC	49	V4	ı	Gamma correction voltage reference
52 V1 I Gamma correction voltage reference 53 GND P Digital ground 54 VDD P Digital power 55 GND P Digital ground 56 VGH P Positive power for TFT 57 VDD P Digital power for Gate IC 58 VGL P Negative power for TFT 59 GND P Digital ground for Gate IC	50	V3	I	Gamma correction voltage reference
53 GND P Digital ground  54 VDD P Digital power  55 GND P Digital ground  56 VGH P Positive power for TFT  57 VDD P Digital power for Gate IC  58 VGL P Negative power for TFT  59 GND P Digital ground for Gate IC	51	V2	I	Gamma correction voltage reference
54 VDD P Digital power  55 GND P Digital ground  56 VGH P Positive power for TFT  57 VDD P Digital power for Gate IC  58 VGL P Negative power for TFT  59 GND P Digital ground for Gate IC	52	V1		Gamma correction voltage reference
55 GND P Digital ground  56 VGH P Positive power for TFT  57 VDD P Digital power for Gate IC  58 VGL P Negative power for TFT  59 GND P Digital ground for Gate IC	53	GND	Р	Digital ground
56 VGH P Positive power for TFT  57 VDD P Digital power for Gate IC  58 VGL P Negative power for TFT  59 GND P Digital ground for Gate IC	54	VDD	Р	Digital power
57 VDD P Digital power for Gate IC  58 VGL P Negative power for TFT  59 GND P Digital ground for Gate IC	55	GND	Р	Digital ground
58 VGL P Negative power for TFT 59 GND P Digital ground for Gate IC	56	VGH	Р	Positive power for TFT
59 GND P Digital ground for Gate IC	57	VDD	P	Digital power for Gate IC
	58	VGL	P	Negative power for TFT
60 NC - Not connect	59	GND	Р	Digital ground for Gate IC
	60	NC NC	-	Not connect

#### Note::

#### UPDN and SHLR control function

UPDN	SHLR	FUNCTION
0	1	Normal display
0	0	Inverse Left and Right
1	1	Inverse Up and Down
1	0	Inverse Left and Right Inverse Up and Down



#### 7. Optical Characteristics

Item	Symbol	Condition	Min.	Тур.	Max.	Unit	Note
Brightness	Вр	<i>θ</i> =0°	250	300	380	Cd/m <sup>2</sup>	1
Uniformity	⊿Bp	Ф=0°	70	80	-	%	1,2
	3:00		-	70	-		
Viewing	6:00	0	-	50	-		Deg 3
Angle	9:00	Cr≥10	-	70		Deg	
	12:00		-	70	-		
Contrast Ratio	Cr	θ=0°	400	500		A	4
Response Time	T <sub>r</sub> +T <sub>f</sub>	Ф=0°		25	40	ms	5
Color of CIE Coordinate	W         X           y         X           R         X           y         X           y         X           y         X           y         X	θ=0° Φ=0°	Typ -0.05	0.313 0.329 0.601 0.339 0.341 0.597 0.122 0.115	Typ +0.05	- - - -	1,6
Ratio	S		45	50	-	%	

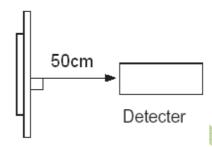
Note: The parameter is slightly changed by temperature, driving voltage and materiel

Note 1: The data are measured after LEDs are turned on for 5 minutes. LCM displays full white. The brightness is the average value of 9 measured spots. Measurement equipment BM-7 (Φ5mm) Measuring condition:

- Measuring surroundings: Dark room.
- Measuring temperature: Ta=25  $^{\circ}$ C.
- Adjust operating voltage to get optimum contrast at the center of the display.



Measured value at the center point of LCD panel after more than 5 minutes while backlight turning on.

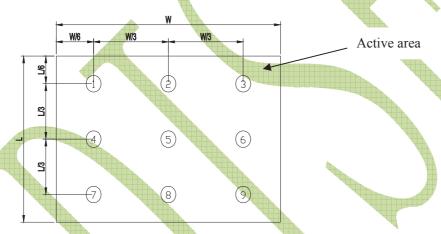


Note 2: The luminance uniformity is calculated by using following formula.

 $\triangle Bp = Bp (Min.) / Bp (Max.) \times 100 (%)$ 

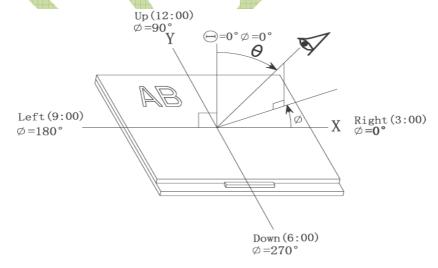
Bp (Max.) = Maximum brightness in 9 measured spots

Bp (Min.) = Minimum brightness in 9 measured spots.

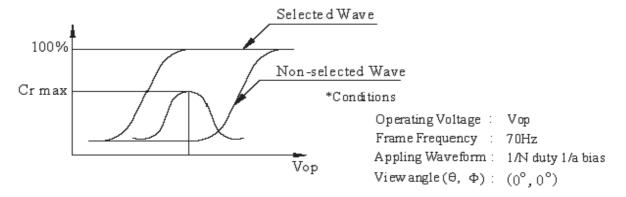


Note 3: The definition of viewing angle:

Refer to the graph below marked by  $\vartheta$  and  $\Phi$ 



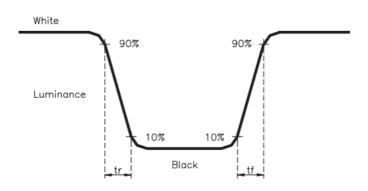
Note 4: Definition of contrast ratio. (Test LCD using DMS501)



Contrast  $ratio(Cr) = \frac{Brightness \ of \ selected \ dots}{Brightness \ of \ non-selected \ dots}$ 

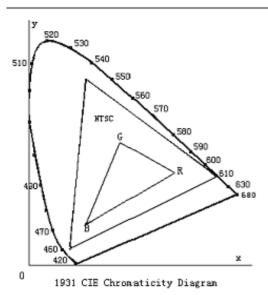
Note 5: Definition of Response time. (Test LCD using DMS501):

The output signals of photo detector are measured when the input signals are changed from "white" to "black" (rising time) and from "black" to "white" (falling time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



The definition of response time

Note 6: Definition of Color of CIE Coordinate and NTSC Ratio.

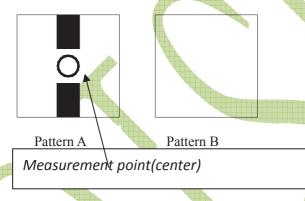


**Color gamut:** 

 $S = \frac{area~of~RGB~triangle}{area~of~NTSC~triangle} \times 100\%$ 

Note 7: Definition of cross talk.

Cross talk ratio(%)=|pattern A Brightness-pattern B Brightness|/pattern A Brightness\*100



Electric volume value=3F+/-3Hex



#### 8. Reliability Test Items and Criteria

No	Test Item	Test condition	Criterion
1	High Temperature Storage	80°C±2°C 96H Restore 2H at 25°C Power off	
2	Low Temperature Storage	-30°C±2°C 96H Restore 2H at 25°C Power off	4. After teeting
3	High Temperature Operation	70°C±2°C 96H Restore 2H at 25°C Power on	1. After testing, cosmetic and electrical defects should not
4	Low Temperature Operation	-20°C±2°C 96H Restore 4H at 25°C Power on	happen. 2. Total current consumption should not be more than twice
5	High Temperature/Humidity Operation	60°C±2°C 90%RH 96H Power on	of initial value.
6	Temperature Cycle	-30°C	

Note: Operation: Supply 3.3V for logic system.

The inspection terms after reliability test, as below

ITEM	Inspection
Contrast	CR>50%
IDD	IDD<200%
Brightness	Brightness>60%
Color Tone	Color Tone+/-0,05

#### 9. Precautions for Use of LCD Modules

#### 9.1 Handling Precautions

- 9.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.
- 9.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.



- 9.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- 9.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.
- 9.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

— Isopropyl alcohol— Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

— Water — Ketone — Aromatic solvents

- 9.1.6 Do not attempt to disassemble the LCD Module.
- 9.1.7 If the logic circuit power is off, do not apply the input signals.
- 9.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
  - a. Be sure to ground the body when handling the LCD Modules.
  - b. Tools required for assembly, such as soldering irons, must be properly ground.
  - c. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
  - d. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

#### 9.2 Storage precautions

- 9.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.
- 9.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature: 0  $^{\circ}$ C  $^{\sim}$  40  $^{\circ}$ C

Relatively humidity: ≤80%

9.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.



**9.3** The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.

