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Revision History

Revision	Date	Remark
1.2	March, 2015	17nm ISATA first release
1.3	March, 2017	15nm ISATA first release
1.4	July, 2017	Function Correction: ISATA DoM doesn't support +5V DC power supply on the 7 th pin.
1.5	Dec., 2017	Error Correction for SLC-type ISATA DoM

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1 Product Overview

1.1 Introduction of DMP ISATA

DMP Serial ATA Disk on Module (SATADOM) ISATA supports SATA III standard (6.0Gb/s) interface with excellent performance and is designed as the smallest form factor size that could enhance compatibility with various design applications. The booting time for operation and the power consumption is less than hard disk drive (HDD). ISATA can work under harsh environment compile with ATA protocol, no additional drives are required, and the SSD can be configured as a boot device or data storage device.

1.2 Product View and Models

DMP ISATA is available in below capacity within MLC/SLC flash ICs.

Standard Temperature Version (0°C ~70°C):

ISATA-8G-H-M	ISATA-1G-H-S	ISATA-8G-H-S
ISATA-16G-H-M	ISATA-2G-H-S	ISATA-16G-H-S
ISATA-32G-H-M	ISATA-4G-H-S	

Wide Temperature Version (-40°C ~+85°C):

ISATA-8G-H-M-X	ISATA-1G-H-S-X	ISATA-8G-H-S-X
ISATA-16G-H-M-X	ISATA-2G-H-S-X	ISATA-16G-H-S-X
ISATA-32G-H-M-X	ISATA-4G-H-S-X	

1.3 SATA Interface

DMP ISATA DoM supports SATA III interface, and compliant with SATA I and SATA II.

2 Product Specifications

2.1 Capacity and Device Parameters

ISATA device parameters are shown in Table 1.

Table 1: Device parameters

Capacity	Cylinders	Heads	Sectors	LBA	User space
1GB	1959	16	63	1974672	964
2GB	3897	16	63	3928176	1918
4GB	7773	16	63	7835184	3826
8GB	15525	16	63	15649200	7,641
16GB	16383	16	63	31277232	15,272
32GB	16383	16	63	62533296	30,534

2.2 Performance

Burst Transfer Rate: 6.0Gbps

Table 2: Performance

ISATA Type MLC					
Capacity	8GB		16GB		32GB
Sequential Read (max.)	100MB/s		100MB/s		100MB/s
Sequential Write (max.)	20MB/s		20MB/s		40MB/s
ISATA Type SLC					
Capacity	1GB	2GB	4GB	8GB	16GB
Sequential Read (max.)	23MB/s	24MB/s	220MB/s	250MB/s	290MB/s
Sequential Write (max.)	9MB/s	18MB/s	50MB/s	60MB/s	120MB/s

Note: the information is based on CrystalDiskMark 3.01 with file size 1000MB test

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2.3 Electrical Specifications

2.3.1 Power Requirement

Table 3: DMP ISATA Power Requirement

Item	Symbol	Rating	Unit
Input voltage	V_{IN}	+5 DC +/- 5%	V

2.3.2 Power Consumption

Table 4: Power Consumption

Mode	Power Consumption (mA)
Read	115 (max.)
Write	110 (max.)
Idle	80 (max.)

* Target: ISATA-16H-M-X

2.4 Environmental Specifications

2.4.1 Temperature Ranges

Table 5: Temperature range for ISATA

Temperature	Range
Operating	Standard Grade: 0°C to 70°C
	Wide-Temperature Grade: -40°C to +85°C
Storage	-55°C to +95°C

2.4.2 Humidity

Relative Humidity: 10-95%, non-condensing

2.4.3 Shock and Vibration

Table 6: Shock/Vibration Testing for ISATA

Reliability	Test Conditions	Reference Standards
Vibration	7 Hz to 2K Hz, 20G, 3 axes	IEC 68-2-6
Mechanical Shock	Duration: 0.5ms, 1500 G, 3 axes	IEC 68-2-27

2.4.4 Mean Time between Failures (MTBF)

Table 7 summarizes the MTBF prediction results for various ISATA configurations. The analysis was performed using a RAM Commander™ failure rate prediction.

- **Failure Rate:** The total number of failures within an item population, divided by the total number of life units expended by that population, during a particular measurement interval under stated condition.
- **Mean Time between Failures (MTBF):** A basic measure of reliability for repairable items: The mean number of life units during which all parts of the item perform within their specified limits, during a particular measurement interval under stated conditions.

Table 7: ISATA-16-H MTBF

Product	Condition	MTBF (Hours)
DMP ISATA	Telcordia SR-332 GB, 25°C	>3,000,000

2.5 CE and FCC Compatibility

DMP ISATA confirmed to CE and FCC requirements.

2.6 RoHS Compliance

DMP ISATA is fully compliant with RoHS directive.

2.7 Reliability

ISATA Type MLC	
Parameter	Value
Read Cycles	Unlimited Read Cycles
Wear-Leveling Algorithm	Support
Bad Blocks Management	Support
Error Correct Code	Support
iData Guard	Support
Thermal Sensor	WT only
Flash endurance	3,000 P/E cycles
TBW* (Total Bytes Written)	
8GB	2.32 (Sequential write)
16GB	4.64 (Sequential write)
32GB	9.28 (Sequential write)
* Total bytes written is based on JEDEC 218 (Solid-State Drive Requirements and Endurance Test Method)	
** Lifespan is calculated by device written per day	

ISATA Type SLC	
Parameter	Value
Read Cycles	Unlimited Read Cycles
Wear-Leveling Algorithm	Support
Bad Blocks Management	Support
Error Correct Code	Support
TBW* (Total Bytes Written)	
1GB	54 (Sequential write)
2GB	108 (Sequential write)
4GB	216 (Sequential write)
8GB	432 (Sequential write)
16GB	864 (Sequential write)

2.8 Transfer Mode

DMP ISATA support following transfer mode:

Serial ATA I 1.5Gbps
 Serial ATA II 3.0Gbps
 Serial ATA III 6.0Gbps

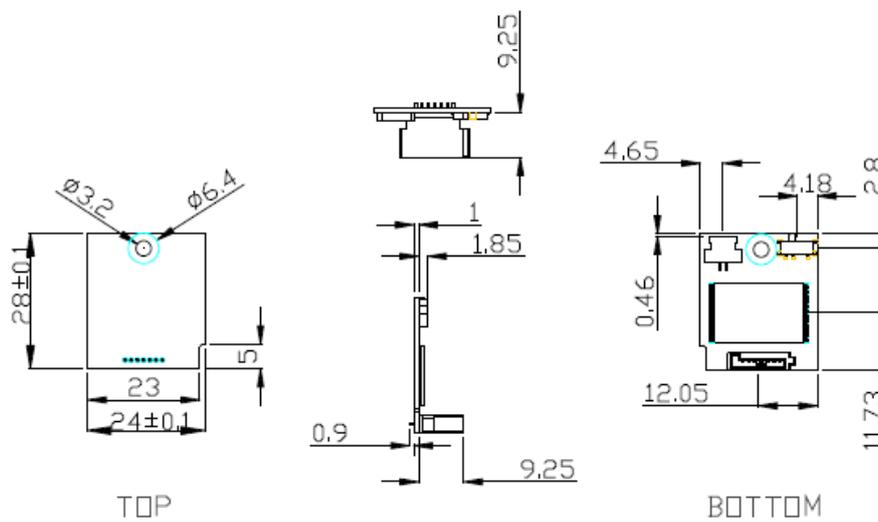
2.9 Pin Assignment

DMP ISATA uses a standard SATA pin-out. See Table 8 for DMP ISATA pin assignment.

Table 8: DMP ISATA Pin Assignment

Name	Type	Description
Pin 1	GND	Shielding
Pin 2	A+	Differential signal to A
Pin 3	A-	Differential signal to A-
Pin 4	GND	Shielding
Pin 5	B-	Differential signal to B-
Pin 6	B+	Differential signal to B
Pin 7	GND	Shielding

2.10 Mechanical Dimensions



Dimension tolerance: ± 0.2 mm

2.11 Assembly Weight

A DMP ISATA within flash ICs, 16GB weight is 7 grams approximately.

2.12 Seek Time

ISATA is not a magnetic rotating design. There is no seek or rotational latency required.

2.13 Hot Plug

The SSD support hot plug function and can be removed or plugged-in during operation. User has to avoid hot plugging the SSD which is configured as boot device and installed operation system.

Surprise hot plug: The insertion of a SATA device into a backplane (combine signal and power) that has power present. The device powers up and initiates an OOB sequence.

Surprise hot removal: The removal of a SATA device from a powered backplane, without first being placed in a quiescent state.

2.14 NAND Flash Memory

DMP ISATA-H-S-X uses Single Level Cell (SLC) NAND flash memory, and DMP ISATA-H-M-X uses Multi Level Cell (MLC) NAND flash memory.

3 Theory of Operation

3.1 Overview

Figure 2 shows the operation of DMP ISATA from the system level, including the major hardware blocks.

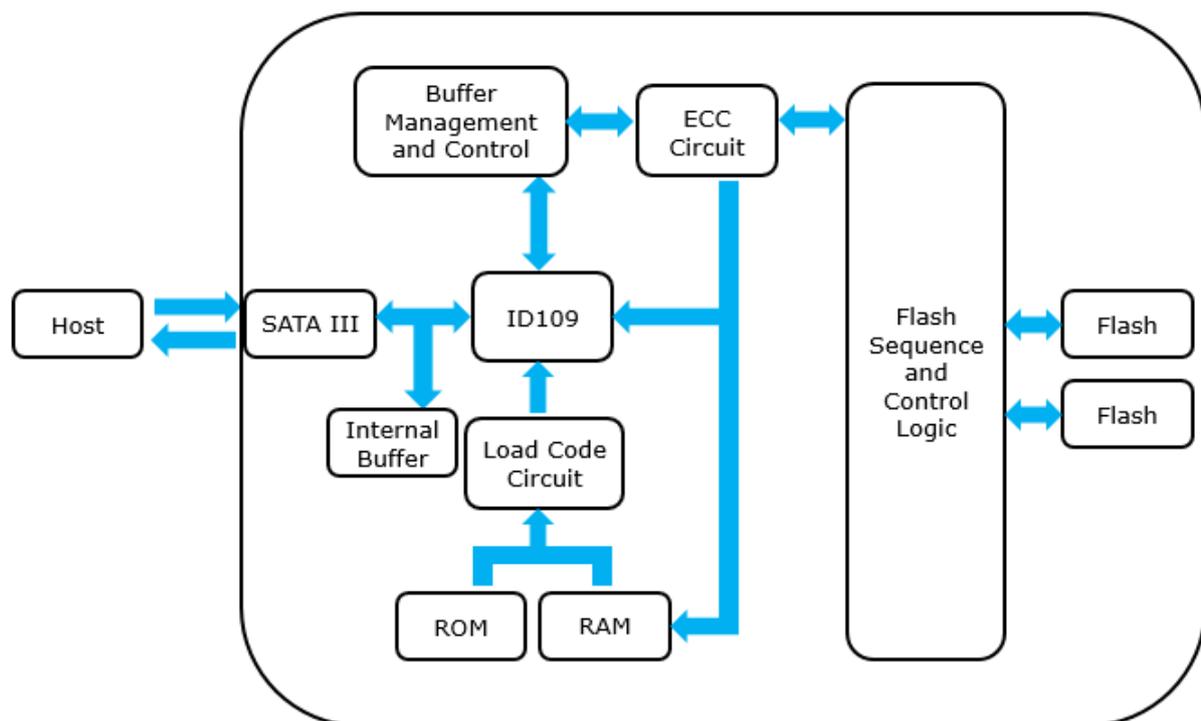


Figure 1: DMP ISATA Block Diagram

DMP ISATA integrates a SATA III controller and NAND flash memories. Communication with the host occurs through the host interface, using the standard ATA protocol. Communication with the flash device(s) occurs through the flash interface.

3.2 SATA III Controller

DMP ISATA is designed with ID 107, a SATA III 6.0Gbps (Gen. 3) controller. The Serial ATA physical, link and transport layers are compliant with Serial ATA Gen 1, Gen 2 and Gen 3 specification (Gen 3 supports 5Gbps/3.0Gbps/6.0Gbps data rate). The controller has 2 channels for flash interface.

3.3 Error Detection and Correction

Highly sophisticated Error Correction Code algorithms are implemented. The ECC unit consists of the Parity Unit (parity-byte generation) and the Syndrome Unit (syndrome-byte computation). This unit implements an algorithm that can correct 40 bits per 1024 bytes in an ECC block. Code-byte generation during write operations, as well as error detection during read operation, is implemented on the fly without any speed penalties.

3.4 Wear-Leveling

Flash memory can be erased within a limited number of times. This number is called the *erase cycle limit* or *write endurance limit* and is defined by the flash array vendor. The erase cycle limit applies to each individual erase block in the flash device.

DMP ISATA uses a static wear-leveling algorithm to ensure that consecutive writes of a specific sector are not written physically to the same page/block in the flash. This spreads flash media usage evenly across all pages, thereby extending flash lifetime.

3.5 Bad Blocks Management

Bad Blocks are blocks that contain one or more invalid bits whose reliability are not guaranteed. The Bad Blocks may be presented while the SSD is shipped, or may develop during the life time of the SSD. When the Bad Blocks is detected, it will be flagged, and not be used anymore. The SSD implement Bad Blocks management, Bad Blocks replacement, Error Correct Code to avoid data error occurred. The functions will be enabled automatically to transfer data from Bad Blocks to spare blocks, and correct error bit.

3.6 Power Cycling

DMP's power cycling management is a comprehensive data protection mechanism that functions before and after a sudden power outage to SSD. Low-power detection terminates data writing before an abnormal power-off, while table-remapping after power-on deletes corrupt data and maintains data integrity. DMP's power cycling provides effective power cycling management, preventing data stored in flash from degrading with use.

3.7 Garbage Collection

Garbage collection is used to maintain data consistency and perform continual data cleansing on SSDs. It runs as a background process, freeing up valuable controller resources while sorting good data into available blocks, and deleting bad blocks. It also significantly reduces write operations to the drive, thereby increasing the SSD's speed and lifespan.

4 Installation Requirements

4.1 DMP ISATA Pin Directions

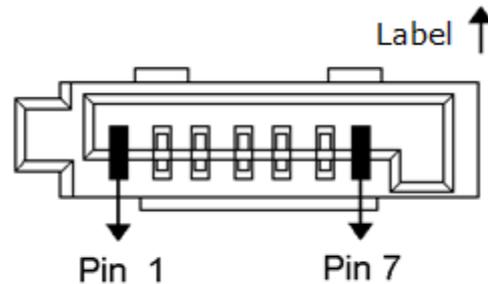


Figure 2: Signal Segment

4.2 Electrical Connections for ISATA

A Serial ATA device may be either directly connected to a host or connected to a host through a cable. For connection via cable, the cable should be no longer than 1meter. The SATA interface has a separate connector for the power supply. Please refer to the pin description for further details.

4.3 Device Drive

No additional device drives are required. The DMP ISATA can be configured as a boot device.