User Manual

M.2(2242) SSD

IM242S Series

Version 1.0

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Revision History

Revision	Description	Date
Rev 1.0	Version 1.0 Released	Jan., 2019

1. Product Overview

1.1 Introduction of ICOP IM242S

ICOP IM242S is characterized by L^3 architecture with the latest SATA III (6.0GHz) Marvell NAND controller. The exclusive L^3 architecture is L^2 architecture multiplied LDPC (Low Density Parity Check). L^2 (Long Life) architecture is a 4K mapping algorithm that reduces WAF and features a real-time wear leveling algorithm to provide high performance and prolong lifespan with exceptional reliability. ICOP IM242S is designed for industrial field, and supports several standard features, including TRIM, NCQ, and S.M.A.R.T. In addition, the exclusive industrial-oriented firmware provides a flexible customization service, making it perfect for a variety of industrial applications.

1.2 Product View and Models

ICOP IM242S is available in follow capacities within MLC flash ICs.

IM242S-8G-M

IM242S-16G-M

IM242S-32G-M

IM242S-64G-M

IM242S-128G-M

IM242S-256G-M

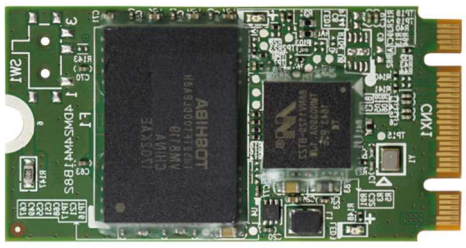
8GB~128GB (TSOP)	256GB (BGA)
	

Figure 1: ICOP IM242S (type 2242)

1.3 SATA Interface

ICOP IM242S supports SATA III interface, and compliant with SATA I and SATA II. SATA III interface can work with Serial Attached SCSI (SAS) host system, which is used in server computer. ICOP IM242S is compliant with Serial ATA Gen 1, Gen 2 and Gen 3 specification (Gen 3 supports 1.5Gbps /3.0Gbps/6.0Gbps data rate).

2. Product Specifications

2.1 Capacity and Device Parameters

IM242S device parameters are shown in Table 1.

Table 1: Device parameters

Capacity	Cylinders	Heads	Sectors	LBA	User Capacity(MB)
8GB	15525	16	63	15649200	7,641
16GB	16383	16	63	31277232	15,272
32GB	16383	16	63	62533296	30,533
64GB	16383	16	63	125045424	61,057
128GB	16383	16	63	250069680	122,104
256GB	16383	16	63	500118192	244,198

2.2 Performance

Burst Transfer Rate: 6.0Gbps

Table 2: Performance

Capacity	8GB	16GB		32GB	64GB	128GB	256GB
		1CH	2CH				
Sequential* Read (max.)	140 MB/s	200 MB/s	270 MB/s	450MB/s	530 MB/s	530 MB/s	530 MB/s
Sequential* Write (max.)	25 MB/s	25 MB/s	60 MB/s	50 MB/s	100 MB/s	120 MB/s	210 MB/s
4KB Random** Read (QD32)	8700 IOPS	10000 IOPS	15000 IOPS	17000 IOPS	27000 IOPS	32000 IOPS	32000 IOPS
4KB Random** Write (QD32)	6900 IOPS	6100 IOPS	14000 IOPS	12000 IOPS	24000 IOPS	29000 IOPS	30000 IOPS

Note: * Sequential performance is based on CrystalDiskMark 5.1.2 with file size 1000MB

** Random performance is based on IO meter with Queue Depth 32

2.3 Electrical Specifications

2.3.1 Power Requirement

Table 3: ICOP IM242S Power Requirement

Item	Symbol	Rating	Unit
Input voltage	V_{IN}	+3.3 DC +- 5%	V

2.3.2 Power Consumption

Table 4: Power Consumption

Mode	Power Consumption (mA)
Startup	818 (max.)
Read	223 (max.)
Write	384 (max.)
Idle	137 (max.)

* Target: 256GB IM242S

2.4 Environmental Specifications

2.4.1 Temperature Ranges

Table 5: Temperature range for IM242S

Temperature	Range
Operating	Standard Grade: 0°C to +70°C
	Industrial Grade:-40°C to +85°C
Storage	-55°C to +95°C

2.4.2 Humidity

Relative Humidity: 10-95%, non-condensing

2.4.3 Shock and Vibration

Table 6: Shock/Vibration Testing for IM242S

Reliability	Test Conditions	Reference Standards
Vibration	7 Hz to 2K Hz, 20G, 3 axes	IEC 68-2-6
Mechanical Shock	Duration: 0.5ms, 1500 G, 3 axes	IEC 68-2-27

2.4.4 Mean Time between Failures (MTBF)

Table 7 summarizes the MTBF prediction results for various IM242S configurations. The analysis was performed using a RAM Commander™ failure rate prediction.

- **Failure Rate**: The total number of failures within an item population, divided by the total number of life units expended by that population, during a particular measurement interval under stated condition.
- **Mean Time between Failures (MTBF)**: A basic measure of reliability for repairable items: The mean number of life units during which all parts of the item perform within their specified limits, during a particular measurement interval under stated conditions.

Table 7: IM242S MTBF

Product	Condition	MTBF (Hours)
ICOP IM242S	Telcordia SR-332 GB, 25°C	>3,000,000

2.5 CE and FCC Compatibility

IM242S conforms to CE and FCC requirements.

2.6 RoHS Compliance

IM242S is fully compliant with RoHS directive.

2.7 Reliability

Table 8: IM242S TBW

Parameter	**Value**	
Read Cycles	Unlimited Read Cycles	
Flash endurance	3,000 P/E cycles	
Wear-Leveling Algorithm	Support	
Bad Blocks Management	Support	
Error Correct Code	Support	
TBW* (Total Bytes Written) Unit: TB		
Capacity	**Sequential workload**	**Client workload**
08GB	23.4	15.6
16GB	46.8	31.2
32GB	93.6	62.4
64GB	187.2	124.8
128GB	374.4	208.3
256GB	748.8	416.6

* Note:

1. Sequential: Mainly sequential write, tested by Vdbench.
2. Client: Follow JESD218 Test method and JESD219A Workload, tested by ULINK. (The capacity lower than 64GB client workload is not specified in JEDEC219A, the values are estimated.)
3. Based on out-of-box performance.

2.8 Transfer Mode

IM242S support following transfer mode:

Serial ATA III 6.0Gbps

Serial ATA II 3.0Gbps

Serial ATA I 1.5Gbps

2.9 Pin Assignment

ICOP IM242S uses a standard SATA pin-out. See Table 9 for IM242S pin assignment.

Table 9: ICOP IM242S Pin Assignment

Signal Name	Pin #	Pin #	Signal Name
		75	GND
3.3V	74	73	GND
3.3V	72	71	GND
3.3V	70	69	GND
NC	68	67	NC
Notch	66	65	Notch
Notch	64	63	Notch
Notch	62	61	Notch
Notch	60	59	Notch
NC	58		
NC	56	57	GND
NC	54	55	NC
NC	52	53	NC
NC	50	51	GND
NC	48	49	RX+
NC	46	47	RX-
NC	44	45	GND
NC	42	43	TX-
NC	40	41	TX+
DEVSLP	38	39	GND
NC	36	37	NC
NC	34	35	NC
NC	32	33	GND
NC	30	31	NC
NC	28	29	NC
NC	26	27	GND
NC	24	25	NC
NC	22	23	NC
NC	20	21	GND
Notch	18	19	Notch
Notch	16	17	Notch
Notch	14	15	Notch
Notch	12	13	Notch
DAS/DSS	10	11	NC

NC	8	9	NC
NC	6	7	NC
3.3V	4	5	NC
3.3V	2	3	GND
		1	GND

2.10 Mechanical Dimensions

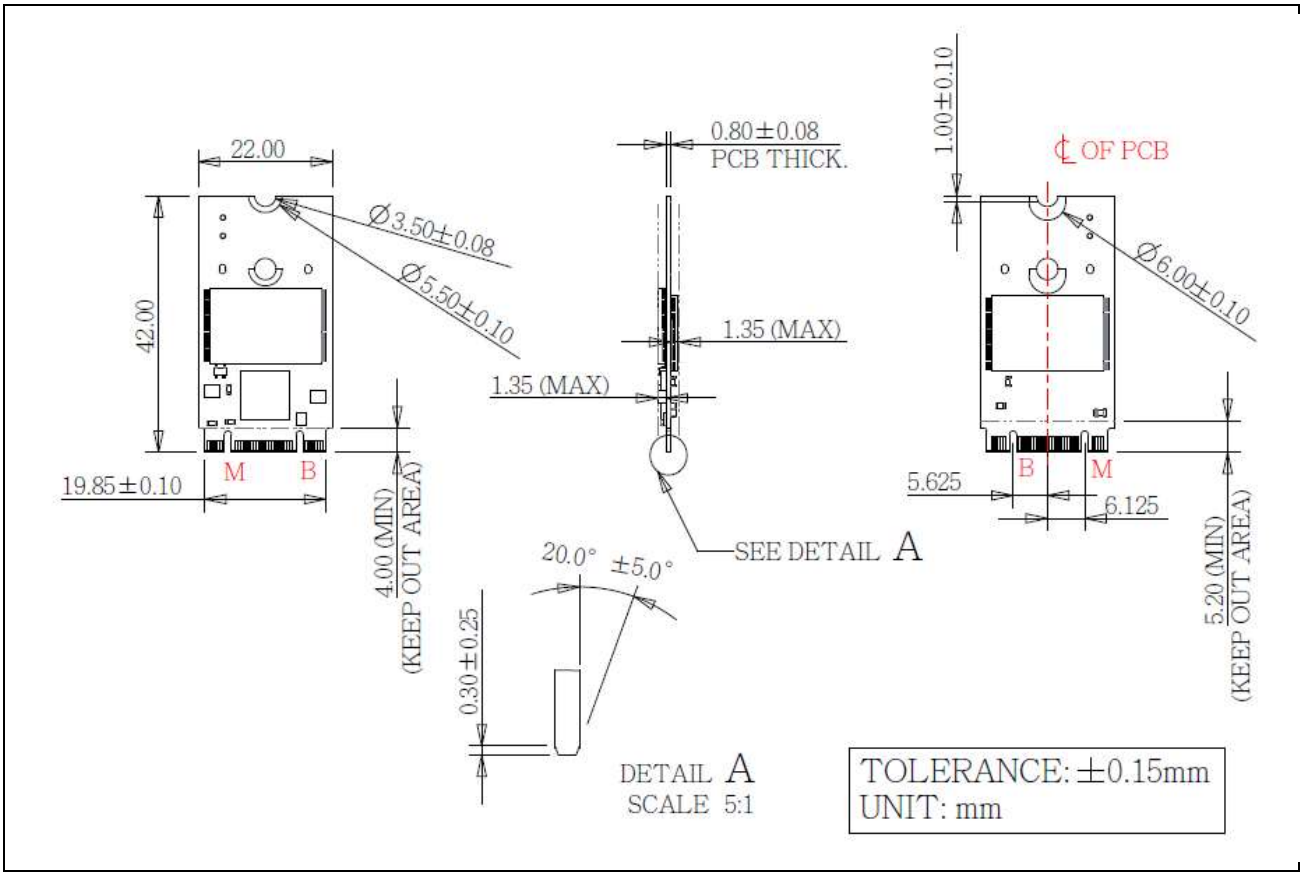


Figure 2: ICOP IM242S diagram (TSOP)

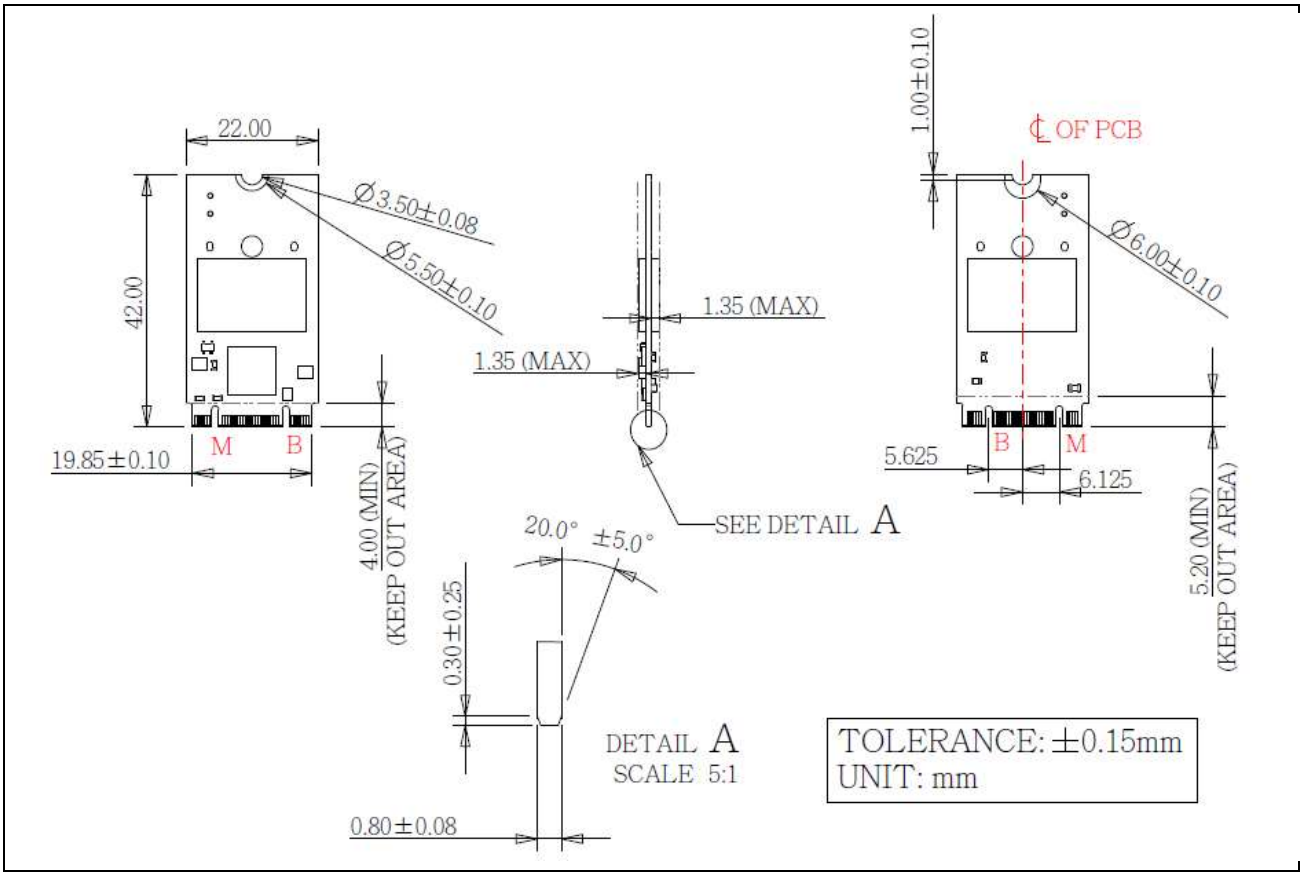


Figure 3: ICOP IM242S diagram (BGA)

2.11 Assembly Weight

A ICOP IM242S within flash ICs, 64GB's weight is 8 grams approximately.

2.12 Seek Time

ICOP IM242S is not a magnetic rotating design. There is no seek or rotational latency required.

2.13 Hot Plug

The SSD support hot plug function and can be removed or plugged-in during operation. User has to avoid hot plugging the SSD which is configured as boot device and installed operation system.

Surprise hot plug : The insertion of a SATA device into a backplane (combine signal and power) that has power present. The device powers up and initiates an OOB sequence.

Surprise hot removal: The removal of a SATA device from a powered backplane, without first being placed in a quiescent state.

2.14 NAND Flash Memory

ICOP IM242S uses Multi Level Cell (MLC) NAND flash memory, which is non-volatility, high reliability and high speed memory storage.

3. Theory of Operation

3.1 Overview

Figure 2 shows the operation of ICOP IM242S from the system level, including the major hardware blocks.

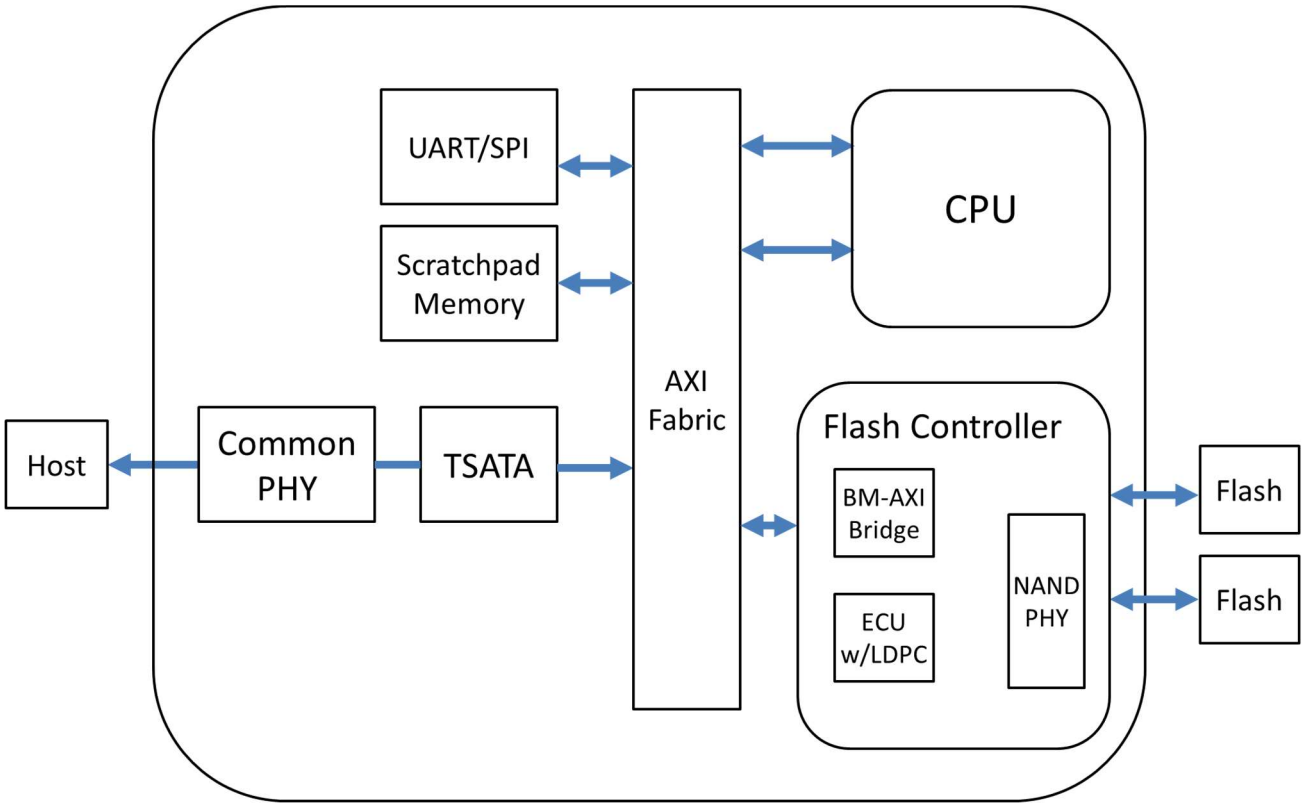


Figure 4: ICOP IM242S Block Diagram

ICOP IM242S integrates a SATA III controller and NAND flash memories. Communication with the host occurs through the host interface, using the standard ATA protocol. Communication with the flash device(s) occurs through the flash interface.

3.2 SATA III Controller

ICOP IM242S is designed with 88NV1120, a SATA III 6.0Gbps (Gen. 3) controller. The Serial ATA physical, link and transport layers are compliant with Serial ATA Gen 1, Gen 2 and Gen 3 specification (Gen 3 supports 1.5Gbps/3.0Gbps/6.0Gbps data rate). The controller has 2 channels for flash interface.

3.3 Error Detection and Correction

ICOP 2.5”SATA SSD 3ME4 is designed with hardware LDPC ECC engine with hard-decision and soft-decision decoding. Low-density parity-check (LDPC) codes have excellent error correcting

performance close to the Shannon limit when decoded with the belief-propagation (BP) algorithm using soft-decision information.

3.4 Wear-Leveling

Flash memory can be erased within a limited number of times. This number is called the ***erase cycle limit*** or ***write endurance limit*** and is defined by the flash array vendor. The erase cycle limit applies to each individual erase block in the flash device.

ICOP IM242S uses a static wear-leveling algorithm to ensure that consecutive writes of a specific sector are not written physically to the same page/block in the flash. This spreads flash media usage evenly across all pages, thereby extending flash lifetime.

3.5 Bad Blocks Management

Bad Blocks are blocks that contain one or more invalid bits whose reliability are not guaranteed. The Bad Blocks may be presented while the SSD is shipped, or may develop during the life time of the SSD. When the Bad Blocks is detected, it will be flagged, and not be used anymore. The SSD implement Bad Blocks management, Bad Blocks replacement, Error Correct Code to avoid data error occurred. The functions will be enabled automatically to transfer data from Bad Blocks to spare blocks, and correct error bit.

3.6 Power Cycling

ICOP's power cycling management is a comprehensive data protection mechanism that functions before and after a sudden power outage to SSD. Low-power detection terminates data writing before an abnormal power-off, while table-remapping after power-on deletes corrupt data and maintains data integrity. ICOP's power cycling provides effective power cycling management, preventing data stored in flash from degrading with use.

3.7 Garbage Collection

Garbage collection is used to maintain data consistency and perform continual data cleansing on SSDs. It runs as a background process, freeing up valuable controller resources while sorting good data into available blocks, and deleting bad blocks. It also significantly reduces write operations to the drive, thereby increasing the SSD's speed and lifespan.

4. Installation Requirements

4.1 IM242S Pin Directions

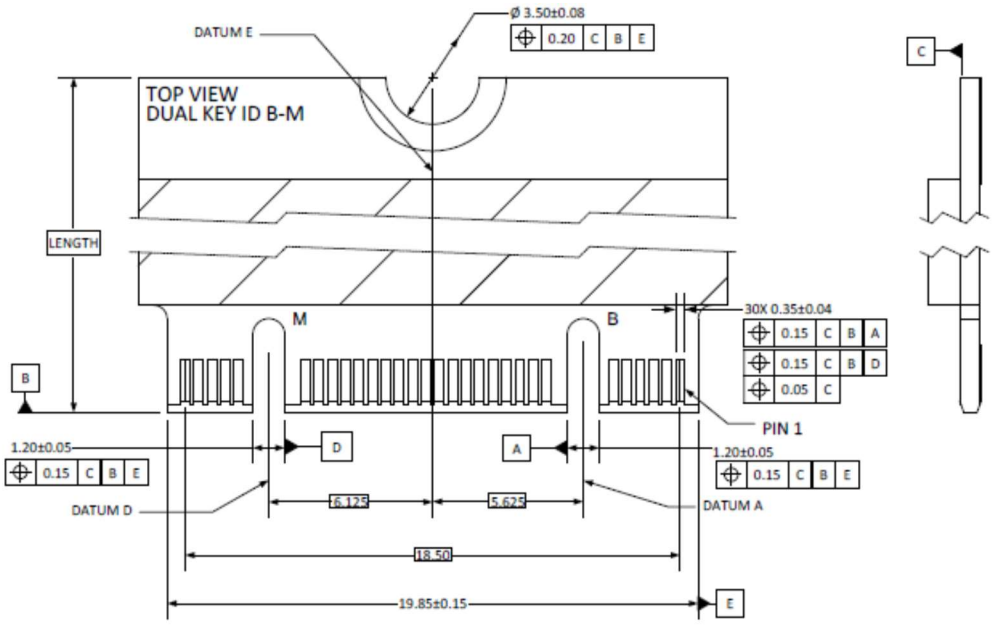


Figure 5: Signal Segment and Power Segment

4.2 Electrical Connections for IM242S

A Serial ATA device may be either directly connected to a host or connected to a host through a cable. For connection via cable, the cable should be no longer than 1meter. The SATA interface has a separate connector for the power supply. Please refer to the pin description for further details.

4.3 Device Drive

No additional device drives are required. The ICOP IM242S can be configured as a boot device.