



ICOP-0101-V2

PC/104 48 Bit Digital I/O Module

Version 1.0

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Revision History

Revision	Date	Remark
1.0	June, 2024	First version release

Table of Contents

1	(General Information	4
	1.1	Description	4
	1.2	Specifications	5
	1.3	Ordering Information	5
	1	3.1 Part No.	5
	1	3.2 Packing List	5
2	I	Hardware Information	6
	2.1	Connector Location	6
	2.2	Connector and Jumper Summary	7
	2.3	Pin Assignments & Jumper Settings	7
	JF	P1 and JP2: IRQ Mode	7
	JF	P3 and JP4: IRQ Level Select	8
	JF	P5 and JP6: IRQ Select	8
	C	ONT9: Digital I/O Group 1	9
	C	ONT10: Digital I/O Group 2	10
	SV	W1: Base Address Setting	11
	C	ONT1: PC/104 Connector – 64 pin	12
	C	ONT2: PC/104 Connector – 40 pin	13
3	(Operational Description	14
	3.1	Mode 0 Operation	14
	3.2	I/O port Assignments	15
	3.3	8255 Data Registers	16
	3.4	8255 Data Mode Registers	17
W	Varr	anty	18

1 General Information

1.1 Description

The ICOP-0101-V2 is a 48-bit digital I/O module. The module can be used together with TTL level input /output circuitry. Its 48 bits are arranged in two 24-bit digital I/O groups. Each group emulates an 8255 PPI (programmable peripheral interface) mode 0, but has a higher driving capacity than the 8255 PPI. Each 24-bit group is divided into three 8-bit ports. A port can be configured to function as input or output.

- 48 digital I/O lines (2 groups)
- Group emulates 8225 PPI mode 0
- Buffered circuits for higher driving capacity than 8255 PPI
- Bit 0 of port C can generate an interrupt to IRQ 2, 3, 4, 5, 6, 7
- Interrupt trigger on rising / falling edge
- Output status readback
- Pin-compatible with OPTO-22 I/O module racks
- Transfer rate: 300 KB/sec. (typical)
- Digital output:

Logic level 0: 0.5 V max. @ 24 mA sink

Logic level 1: 2.0 V min. @ 15 mA source

Digital input:

Logic level 0: 0.8 V max.

Logic level 1: 2.0 V min.

1.2 Specifications

Bus	PC/104 Standard Compliant	
I/O Interface	24-bit Digital I/O x2	
Connectors	2.54mm 50-pin box header for I/O port x2	
Power	DC 15V @220m A (Typical)	
Requirement	DC +5V @220mA (Typical)	
Weight	80g	
Dimensions	90mm x 96mm (3.54 x 3.77 inches)	
Operating Temp.	$-20^{\circ}\text{C} \sim +70^{\circ}\text{C}$	

1.3 Ordering Information

1.3.1 Part No.

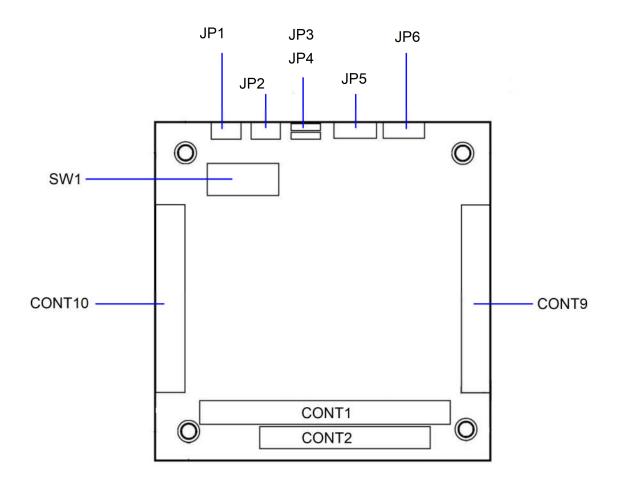
• ICOP-0101-V2

1.3.2 Packing List

- ICOP-0101-V2 x1
- Screw Kit x1

2 Hardware Information

2.1 Connector Location



2.2 Connector and Jumper Summary

Nbr.	Name	Type of Connections	Nbr of Pin
JP1	IRQ Mode	Pin Header, 2.54mm, 2x3	6
JP2	IRQ Mode	Pin Header, 2.54mm, 2x3	6
JP3	IRQ Level Select	Pin Header, 2.54mm, 1x3	3
JP4	IRQ Level Select	Pin Header, 2.54mm, 1x3	3
JP5	IRQ Select	Pin Header, 2.54mm, 2x6	12
JP6	IRQ Select	Pin Header, 2.54mm, 2x6	12
CONT9	Digital I/O Group 1	Pin Header, 2.54mm, 2x25	50
CONT10	Digital I/O Group 2	Pin Header, 2.54mm, 2x25	50
SW1	Base Address Setting	Dip switch	
CONT1	PC/104 Connector – 64 pin	Box Header, 2.54mm, 32x2	64
CONT2	PC/104 Connector – 40 pin	Box Header, 2.54mm, 20x2	40

2.3 Pin Assignments & Jumper Settings

JP1 and JP2: IRQ Mode

The interrupt function can be enabled (INT) or disabled (DIS) by jumper setting. A third option, a more dynamic approach, is to choose for an external device to enable/disable the interrupt function (EXT).

Although you can only make one choice for both groups, the groups interrupt function can be enabled/disabled separately when you choose for the EXT setting. Line PC04 and PC14 control the mode of interrupt for PC00 and PC10. TTL Low disables an interrupt and TTL High enables an interrupt.



JP3 and JP4: IRQ Level Select

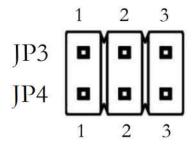
JP3 and JP4 control the trigger edge (rising or falling) on both pin PC00 (JP3) and PC10 (JP4).

Rising edge: an interrupt will be generated when the I/O line (PC00 or PC10) changes from TTL Low to TTL High.

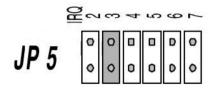
Falling edge: an interrupt will be generated when the I/O line (PC00 or PC10) changes from TTL High to TTL Low.

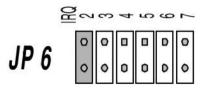
In the situation on the right(PIN2&PIN3) the interrupt is set to be triggered on the rising edge.

In the situation on the left(PIN1&PIN2) the interrupt is set to be triggered on the falling edge.



JP5 and JP6: IRQ Select





CONT9: Digital I/O Group 1

Pin	Description		Description
1	PC07	2	GND
3	PC06	4	GND
5	PC05	6	GND
7	PC04	8	GND
9	PC03	10	GND
11	PC02	12	GND
13	PC01	14	GND
15	PC00	16	GND
17	PB07	18	GND
19	PB06	20	GND
21	PB05	22	GND
23	PB04	24	GND
25	PB03	26	GND
27	PB02	28	GND
29	PB01	30	GND
31	PB00	32	GND
33	PA07	34	GND
35	PA06	36	GND
37	PA05	38	GND
39	PA04	40	GND
41	PA03	42	GND
43	PA02	44	GND
45	PA01	46	GND
47	PA00	48	GND
49	+5V	50	GND

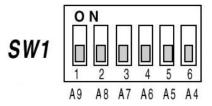
CONT10: Digital I/O Group 2

Pin	Description	Pin	Description
1	PC17	2	GND
3	PC16	4	GND
5	PC15	6	GND
7	PC14	8	GND
9	PC13	10	GND
11	PC12	12	GND
13	PC11	14	GND
15	PC10	16	GND
17	PB17	18	GND
19	PB16	20	GND
21	PB15	22	GND
23	PB14	24	GND
25	PB13	26	GND
27	PB12	28	GND
29	PB11	30	GND
31	PB10	32	GND
33	PA17	34	GND
35	PA16	36	GND
37	PA15	38	GND
39	PA14	40	GND
41	PA13	42	GND
43	PA12	44	GND
45	PA11	46	GND
47	PA10	48	GND
49	+5V	50	GND

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SW1: Base Address Setting

The ICOP-0101-V2 occupies 8 consecutive I/O locations and Dip-switch SW1 sets the base address for it. Be careful when selecting the base address as some settings can conflict with existing PC ports. The following table shows common examples that usually will not cause a conflict



Hex	1	2	3	4	5	6		
000-00F	ON	ON	ON	ON	ON	ON		
010-01F	ON	ON	ON	ON	ON	OFF		
200-20F	OFF	ON	ON	ON	ON	ON		
210-21F	OFF	ON	ON	ON	ON	OFF		
300-30F	OFF	OFF	ON	ON	ON	ON		
3F0-3FF	OFF	OFF	OFF	OFF	OFF	OFF		

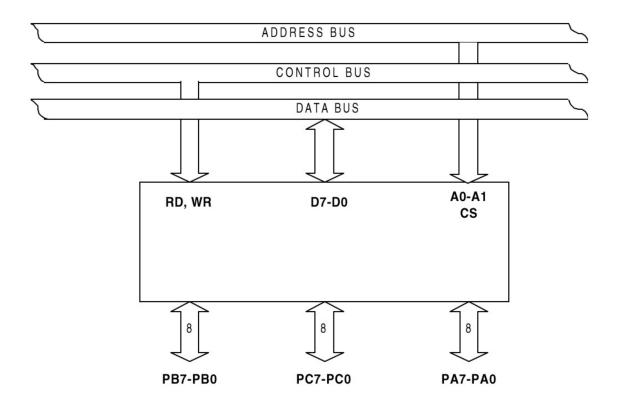
CONT1: PC/104 Connector – 64 pin

Pin#	Single Name	Pin#	Single Name
1.	IOCHCHK*	2	GND
3	SD7 4 RI		RESETDRV
5	SD6 6		VCC
7	SD5	8	IRQ9
9	SD4	10	-5V
11	SD3	12	RDQ2
13	SD2	14	-12V
15	SD1	16	OWS
17	SD0	18	+12V
19	IOCHRDY	20	GND
21	AEN	22	SMEMW*
23	SA19	24	SMEMR*
25	SA18	26	IOW*
27	SA17	28	IOR*
29	SA16	30	DACK3*
31	SA15	32	DRQ3
33	SA14	34	DACK1*
35	SA13	36	DRQ1*
37	SA12	38	REFRESH*
39	SA11	40	SYSCLK
41	SA10	42	IRQ7
43	SA9	44	IRQ6
45	SA8	46	IRQ5
47	SA7	48	IRQ4
49	SA6	50	IRQ3
51	SA5	52	DACK2*
53	SA4	54	TC
55	SA3	56	BALE
57	SA2	58	VCC
59	SA1	60	OSC
61	SA0	62	GND
63	GND	64	GND

CONT2: PC/104 Connector – 40 pin

Pin#	Single Name	Pin#	Single Name
1.	GND	2	GND
3	MEMCS16*	4	SBHE*
5	IOCS16*	6	SA23
7	IRQ10	8	SA22
9	IRQ11	10	SA21
11	IRQ12	12	SA20
13	IRQ15	14	SA19
15	IRQ14	16	SA18
17	17 DACK0*		SA17
19	DRQ0	20	MEMR*
21	DACK5*	22	MEMW*
23	DRQ5	24	SD8
25	DACK6*	26	SD9
27	DRQ6	28	SD10
29	DACK7	30	SD11
31	DRQ7	32	SD12
33	VCC	34	SD13
35	MASTER*	36	SD14
37	GND	38	SD15
39	GND	40	NC

3 Operational Description



3.1 Mode 0 Operation

Mode 0 operation provides simple input and output operation for each of the three ports. No handshaking is required. Data is simply written to or read from a specific port.

Mode 0 Basic Functional Definitions:

- Three 8-bit ports
- Any port can be input or output
- Outputs are latched
- Inputs are not latched

3.2 I/O port Assignments

_	_	
Location	Write	Read
Base+0	Α0	A0
Base+1	В0	В0
Base+2	CO	CO
Base+3	Mode Register for A0, B0, C0	N/A
Base+4	A1	A1
Base+5	B1	B1
Base+6	C1	C1
Base+7	Mode Register for A1, B1, C1	N/A

3.3 8255 Data Registers

Base+0 Port A0 (read/write)

Bit	7	6	5	4	3	2	1	0
Value	PA07	PA06	PA05	PA04	PA03	PA02	PA01	PA00

Base+1 Port B0 (read/write)

Bit	7	6	5	4	3	2	1	0
Value	PB07	PB06	PB05	PB04	PB03	PB02	PB01	PB00

Base+2 Port C0 (read/write)

Bit	7	6	5	4	3	2	1	0
Value	PC07	PC06	PC05	PC04	PC03	PC02	PC01	PC00

Base+4 Port A1 (read/write)

Bit	7	6	5	4	3	2	1	0
Value	PA17	PA16	PA15	PA14	PA13	PA12	PA11	PA10

Base+5 Port B1 (read/write)

Bit	7	6	5	4	3	2	1	0
Value	PB17	PB16	PB15	PB14	PB13	PB12	PB11	PB10

Base+6 Port C1 (read/write)

Bit	7	6	5	4	3	2	1	0
Value	PC17	PC16	PC15	PC14	PC13	PBC2	PC11	PC10

3.4 8255 Data Mode Registers

Base+3 Port A0, B0, C0 (write)

Bit	7	6	5	4	3	2	1	0
Value	1	0	0	PA0	PC0	0	PB0	PC0
					(upper)			(lower)

PA0=0 → Port A0 is oupput

 $PA0=1 \rightarrow Port A0 is input$

PB0=0 \rightarrow Port B0 is oupput

PB0=1 → Port B0 is input

 $PC0=0 \rightarrow Port C0 is oupput$

 $PC0=1 \rightarrow Port C0 is input$

Base+7 Port A1, B1, C1 (write)

Bit	7	6	5	4	3	2	1	0
Value	1	0	0	PA1	PC1	0	PB1	PC1
					(upper)			(lower)

PA1=0 \rightarrow Port A1 is oupput

PA1=1 → Port A1 is input

PB1=0 → Port B1 is oupput

PB1=1 → Port B1 is input

PC1=0 \rightarrow Port C1 is oupput

PC1=1 \rightarrow Port C1 is input

Note:

After power-on or reset of the module the A0, B0, C0, A1, B1 and C1 ports are default set to input mode!

Warranty

This product is warranted to be in good working order for a period of one year (12 months) from the date of purchase. Should this product fail to be in good working order at any time during this period, we will, at our option, replace or repair it without additional charge except as set forth in the following terms. This warranty does not apply to products damaged by misuse, modifications, accident or disaster. Vendor assumes no liability for any damages, lost profits, lost savings or any other incidental or consequential damage resulting from the use, misuse of, originality to use this product. Vendor will not be liable for any claim made by any other related party. Return authorization must be obtained from the vendor before returned merchandise is accepted. Authorization can be obtained by calling or faxing the vendor and requesting a Return Merchandise Authorization (RMA) number. Returned goods should always be accompanied by a clear problem description. Should you have questions about warranty and RMA service, please contact us directly.

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